

LCFC Confidential


Y530 M/B Schematics Document

Coffee Lake H-Processor with DDR4 + NV N17P-G0/G1 GPU


XXXXXX

2017-09-11

REV: 0.1

Security Classification	LC Future Center Secret Data			Title	 Cover Page
Issued Date	2015/02/26	Deciphered Date	2016/02/26	Size	
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				Custom	EY515
				Date:	Tuesday, March 20, 2018
				Sheet	1 of 74
				Rev	1.0

[illegible]

Security Classification	LC Future Center Secret Data		Title	 Block Diagram
Issued Date	2015/02/26	Deciphered Date	2016/02/26	
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Doc #	Document Number		Rev 1.0	
Date	Issued, March 20, 2018		Rev 1.0	
			Sheet	2 of 4

Power Plane State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCC10 VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_AON +1.8VGS NVVDD NVVDDS +1.0VGS FBVDDQ
S0	○	○	○	○	○
S3	○	○	○	○	✗
S3 Battery only	○	○	○	○	✗
S5 S4/AC Only	○	○	○	✗	✗
S5 S4 Battery only	○	✗	✗	✗	✗
S5 S4 AC & Battery don't exist	✗	✗	✗	✗	✗

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

[illegible]

USB2.0 Port table	
Port	Function
1	Back USB3.0
2	Left USB3.0
3	Right USB3.0
4	Type-C Port
5	NA
6	Camera
7:13	NA
14	BT

Port	Function
1	Back USB3.0
2	Type-C Port
3	Left USB3.0
4	Right USB3.0
5	NA
6	NA

SATA Port table	
Port	Function
0A	NA
0B	NA
1A	M.2 SSD Gen3
1B	NA
2	HDD Gen3
3	NA
4	NA
5	NA

PCIe Port table	
Port	Function
1:8	NA
9	M.2 SSD/Optane
10	M.2 SSD/Optane
11	M.2 SSD/Optane
12	M.2 SSD/Optane
13	WLAN Gen1
14	LAN Gen1
15:24	NA

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Title			
Notes List			
Size	Document Number	Rev	
Custom	EY515	1.0	

[24] PCIE_CRX_GTX_N0..19

[24] PCIE_CRX_GTX_P0..19

PCIE_CTX_C_GRX_N0..19 [24]

PCIE_CTX_C_GRX_P0..19 [24]

VCCIO

Note:
Place R_comp inside CPU cavity
Trace width=12 mils, Spacing=15mil
Max length= 400 mils.

RC1 2

1 24.9 0402 1%

PEG_COMP G2

PEG_RCOMP

[19] DMI_CRX_PTX_P0 DMI_CRX_PTX_N0 DMI_RXP_0 DMI_TXP_0 B8 DMI_CTX_PRX_P0 DMI_CTX_PRX_N0 [19]

[19] DMI_CRX_PTX_P1 DMI_CRX_PTX_N1 DMI_RXP_1 DMI_TXP_1 C6 DMI_CTX_PRX_P1 DMI_CTX_PRX_N1 [19]

[19] DMI_CRX_PTX_P2 DMI_CRX_PTX_N2 DMI_RXP_2 DMI_TXP_2 B5 DMI_CTX_PRX_P2 DMI_CTX_PRX_N2 [19]

[19] DMI_CRX_PTX_P3 DMI_CRX_PTX_N3 DMI_RXP_3 DMI_TXP_3 D4 DMI_CTX_PRX_P3 DMI_CTX_PRX_N3 [19]

COFFEE LAKE-H-CPU_BGA1440

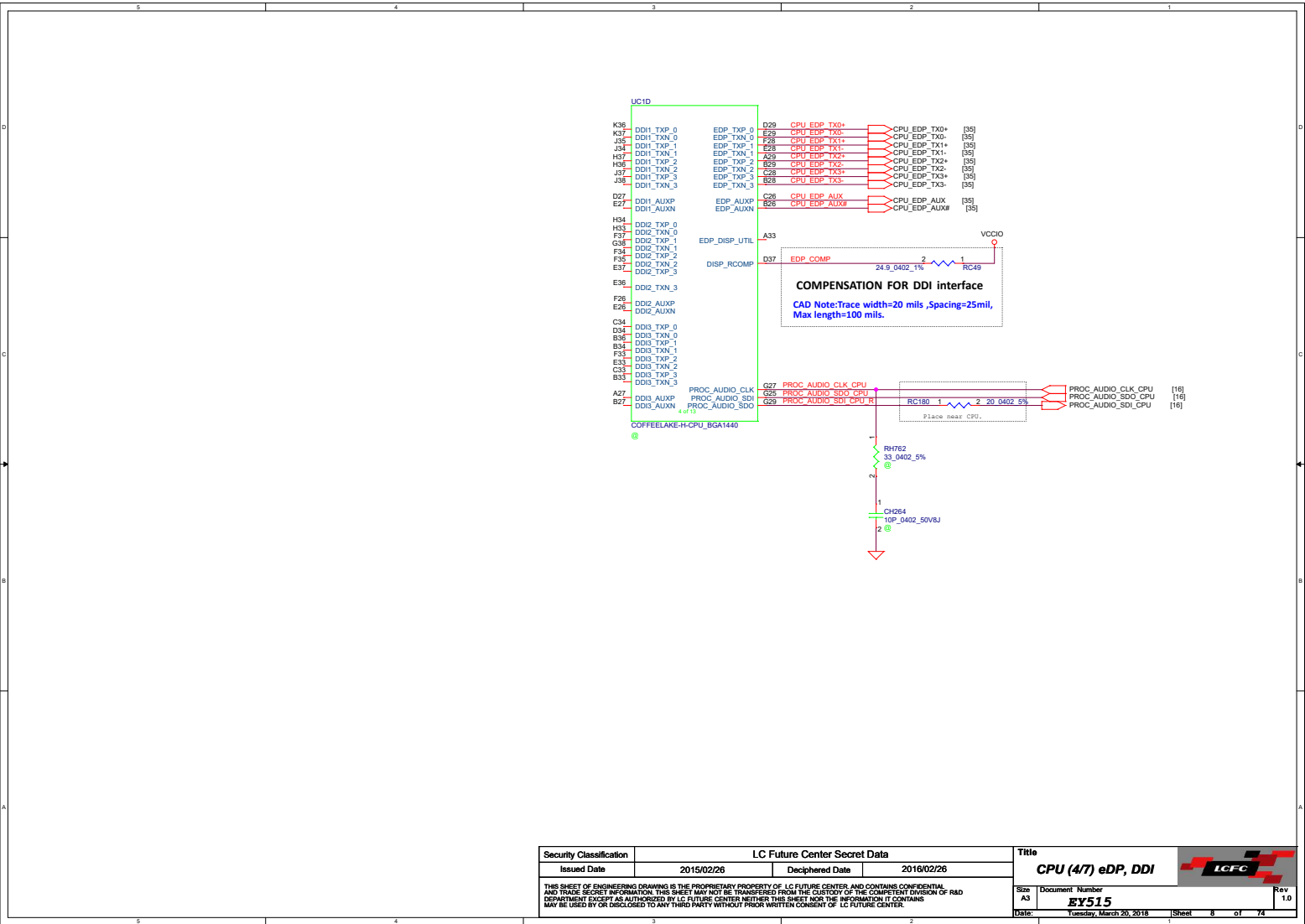
8

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Size Document Number
Customer EY515
Date: Tuesday, March 26, 2018 18sheet 8 of 74
Rev 1.0



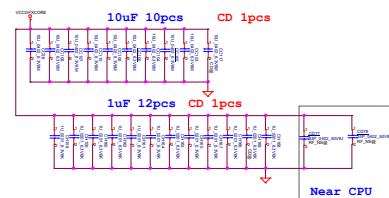
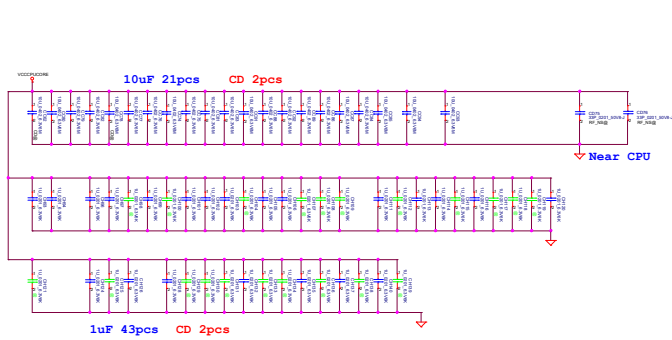
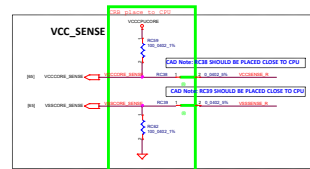
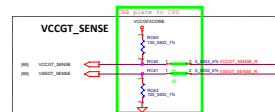
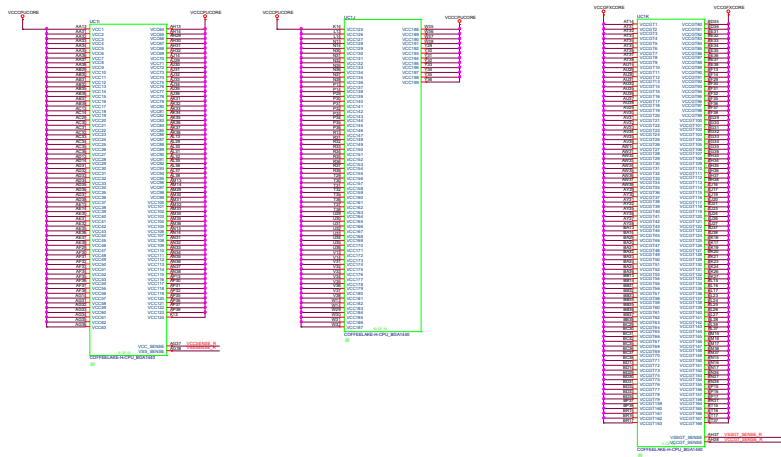


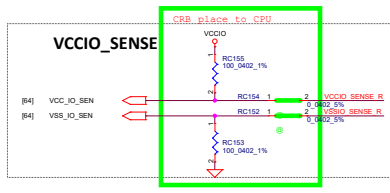
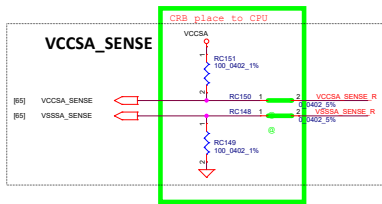
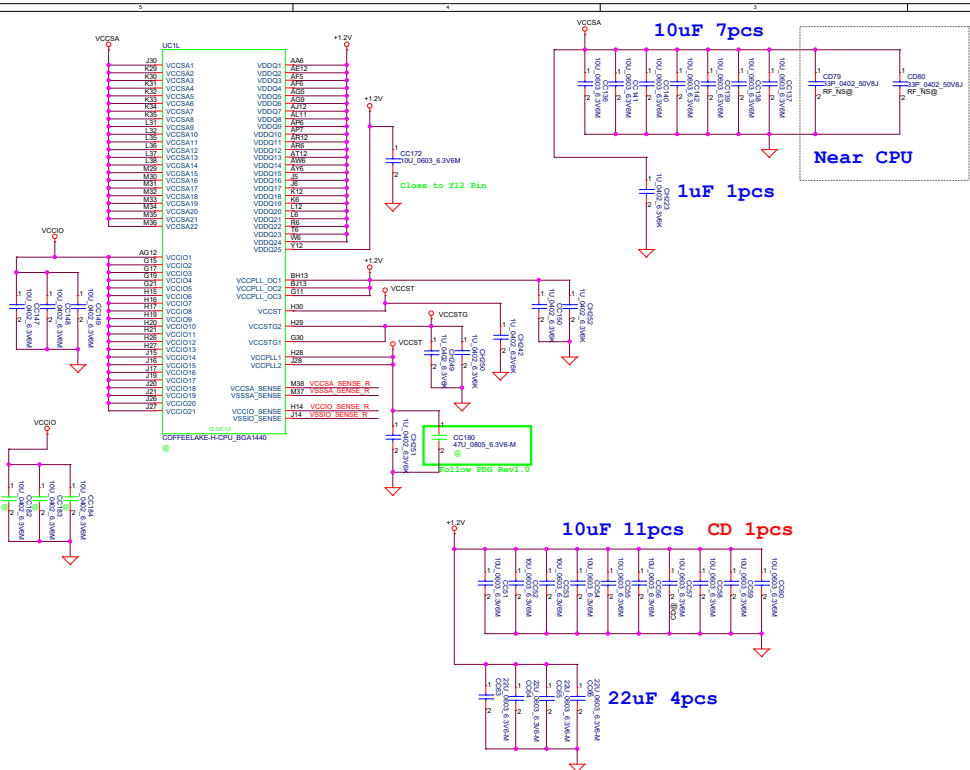



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Document Number		Rev	
A3		1.0	
EY515		1.0	
Date: Tuesday, March 20, 2018		Sheet 8 of 24	








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Size	C		Document Number	EY515			Rev		1.0
Date:	Tuesday, March 26, 2016		Sheet	19		of		24	

UCIF			
A10			A04
A5	V58	1	A10
A18	V58	2	A12
A19	V58	3	A14
A20	V58	4	A15
A25	V58	5	A16
A26	V58	6	A17
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A39	V58	121	A132

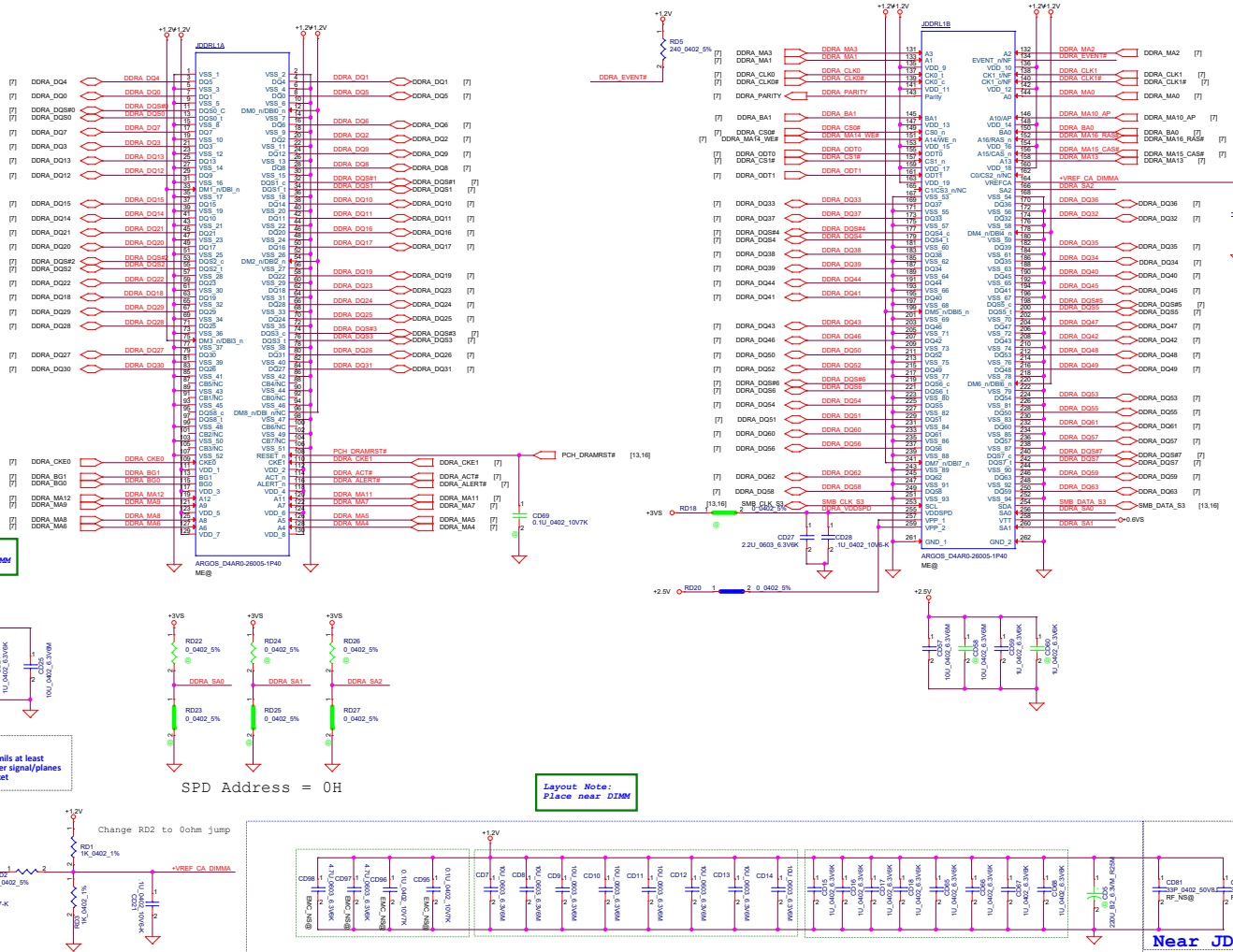
AW5					
BS	VS5	163	VS5	244	B115
A12	VS6	164	VS6	245	B116
AY10	VS6	165	VS6	246	B120
AY11	VS6	166	VS6	247	B121
AY12	VS6	167	VS6	248	B122
AY13	VS6	168	VS6	249	B123
AY14	VS6	169	VS6	250	B124
AY15	VS6	170	VS6	251	B125
BA38	VS7	171	VS7	252	BA38
BA39	VS7	172	VS7	253	BA39
BA40	VS7	173	VS7	254	BA40
BA41	VS7	174	VS7	255	BA41
BA42	VS7	175	VS7	256	BA42
BA43	VS7	176	VS7	257	BA43
BA44	VS7	177	VS7	258	BA44
BA45	VS7	178	VS7	259	BA45
BB12	VS8	179	VS8	260	BB12
BB13	VS8	180	VS8	261	BB13
BB14	VS8	181	VS8	262	BB14
BB15	VS8	182	VS8	263	BB15
BB16	VS8	183	VS8	264	BB16
BB17	VS8	184	VS8	265	BB17
BB18	VS8	185	VS8	266	BB18
BB19	VS8	186	VS8	267	BB19
BB20	VS8	187	VS8	268	BB20
BB21	VS8	188	VS8	269	BB21
BB22	VS8	189	VS8	270	BB22
BB23	VS8	190	VS8	271	BB23
BB24	VS8	191	VS8	272	BB24
BB25	VS8	192	VS8	273	BB25
BB26	VS8	193	VS8	274	BB26
BB27	VS8	194	VS8	275	BB27
BB28	VS8	195	VS8	276	BB28
BB29	VS8	196	VS8	277	BB29
BB30	VS8	197	VS8	278	BB30
BB31	VS8	198	VS8	279	BB31
BB32	VS8	199	VS8	280	BB32
BB33	VS8	200	VS8	281	BB33
BB34	VS8	201	VS8	282	BB34
BB35	VS8	202	VS8	283	BB35
BB36	VS8	203	VS8	284	BB36
BB37	VS8	204	VS8	285	BB37
BB38	VS8	205	VS8	286	BB38
BB39	VS8	206	VS8	287	BB39
BB40	VS8	207	VS8	288	BB40
BB41	VS8	208	VS8	289	BB41
BB42	VS8	209	VS8	290	BB42
BB43	VS8	210	VS8	291	BB43
BB44	VS8	211	VS8	292	BB44
BB45	VS8	212	VS8	293	BB45
BB46	VS8	213	VS8	294	BB46
BB47	VS8	214	VS8	295	BB47
BB48	VS8	215	VS8	296	BB48
BB49	VS8	216	VS8	297	BB49
BB50	VS8	217	VS8	298	BB50
BB51	VS8	218	VS8	299	BB51
BB52	VS8	219	VS8	300	BB52
BB53	VS8	220	VS8	301	BB53
BB54	VS8	221	VS8	302	BB54
BB55	VS8	222	VS8	303	BB55
BB56	VS8	223	VS8	304	BB56
BB57	VS8	224	VS8	305	BB57
BB58	VS8	225	VS8	306	BB58
BB59	VS8	226	VS8	307	BB59
BB60	VS8	227	VS8	308	BB60
BB61	VS8	228	VS8	309	BB61
BB62	VS8	229	VS8	310	BB62
BB63	VS8	230	VS8	311	BB63
BB64	VS8	231	VS8	312	BB64
BB65	VS8	232	VS8	313	BB65
BB66	VS8	233	VS8	314	BB66
BB67	VS8	234	VS8	315	BB67
BB68	VS8	235	VS8	316	BB68
BB69	VS8	236	VS8	317	BB69
BB70	VS8	237	VS8	318	BB70
BB71	VS8	238	VS8	319	BB71
BB72	VS8	239	VS8	320	BB72
BB73	VS8	240	VS8	321	BB73
BB74	VS8	241	VS8	322	BB74
BB75	VS8	242	VS8	323	BB75
B114	VS9	324	VS9	324	B114

COFFEECAN+CPU, BS0440

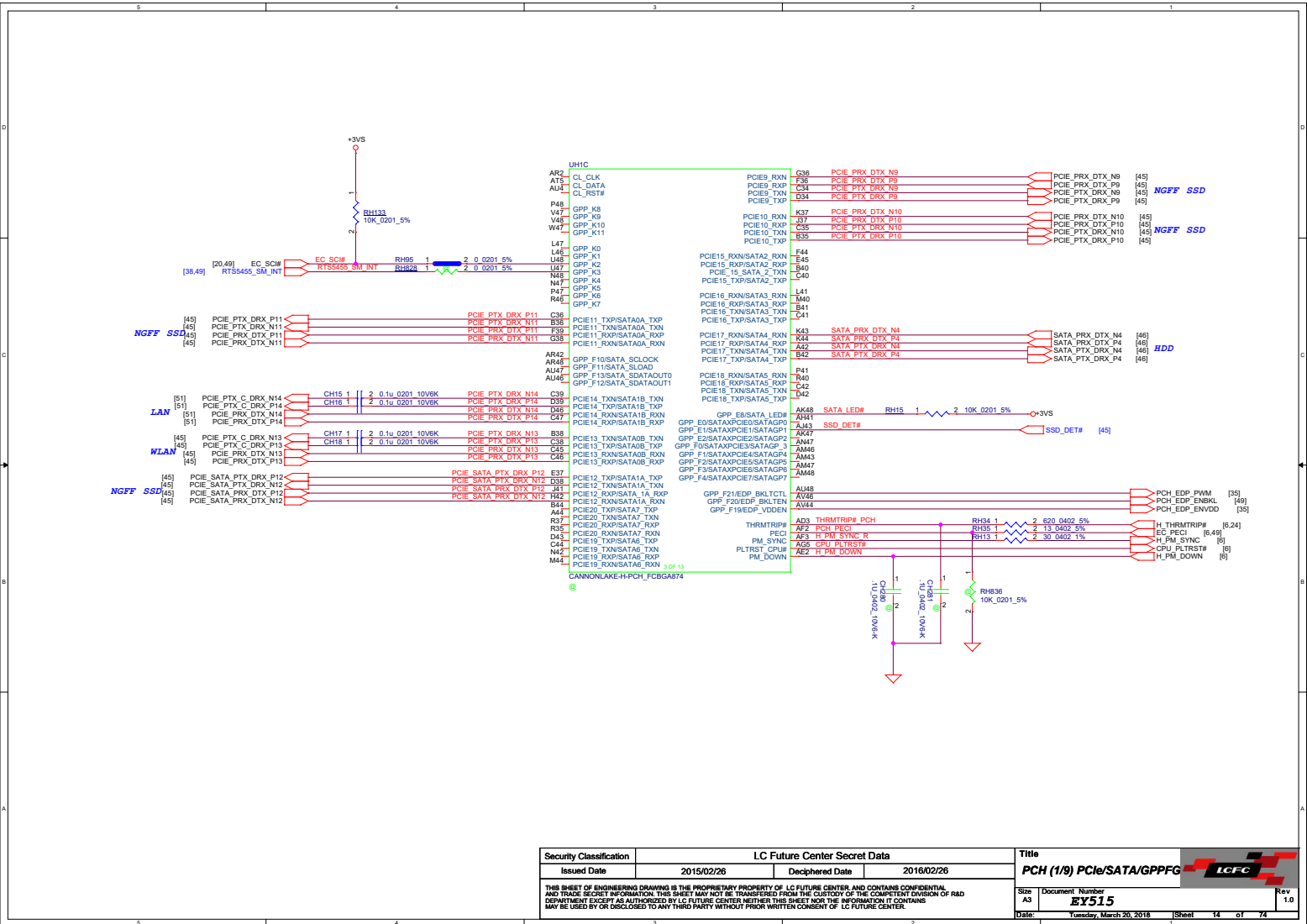
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BM7	355-329	V55	A12
BM8	355-329	V55	A12
BM9	355-330	V55	A13
BM10	355-330	V55	A13
BM11	355-331	V55	A14
BM12	355-331	V55	A14
BM13	355-332	V55	A15
BM14	355-332	V55	A15
BM15	355-333	V55	A16
BM16	355-333	V55	A16
BM17	355-334	V55	A17
BM18	355-335	V55	A18
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BM20	355-336	V55	A19
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BM107	355-384	V55	A67
BM108	35		

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/02/26	Declassified Date	2016/02/26	CPU (6/7) PWR, VSS	
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Date	Tuesday, March 26, 2018		Sheet	11	of 74

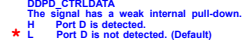
DDR SO-DIMM A




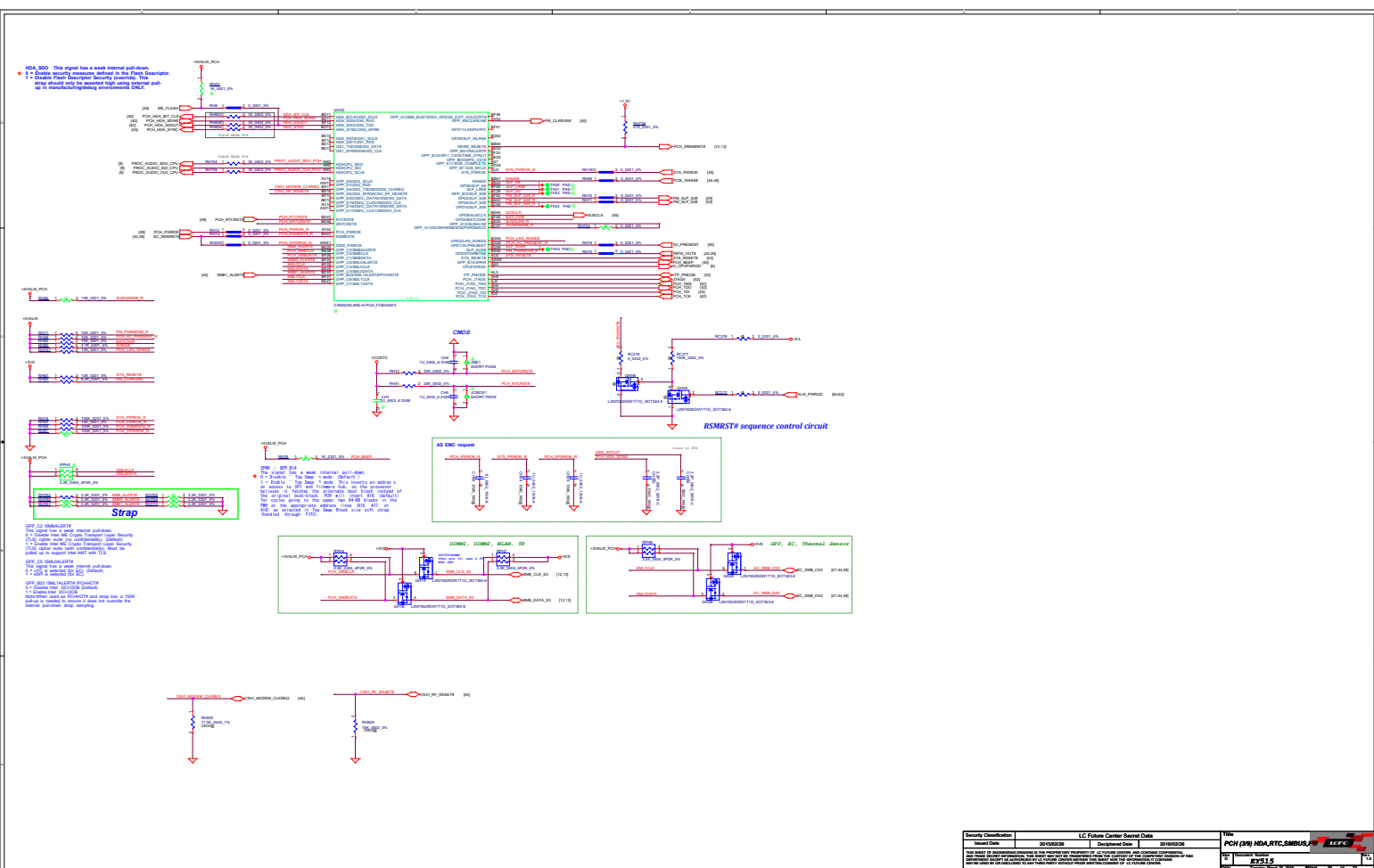
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Issued Date	2015/02/26	Deciphered Date	2016/02/26	DDRVI SO-DIMM A	
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Rev	C	Document Number	EX515	Rev	1.0
DATE	2015/02/26	REVISED	2015/02/26	REVISED	2015/02/26

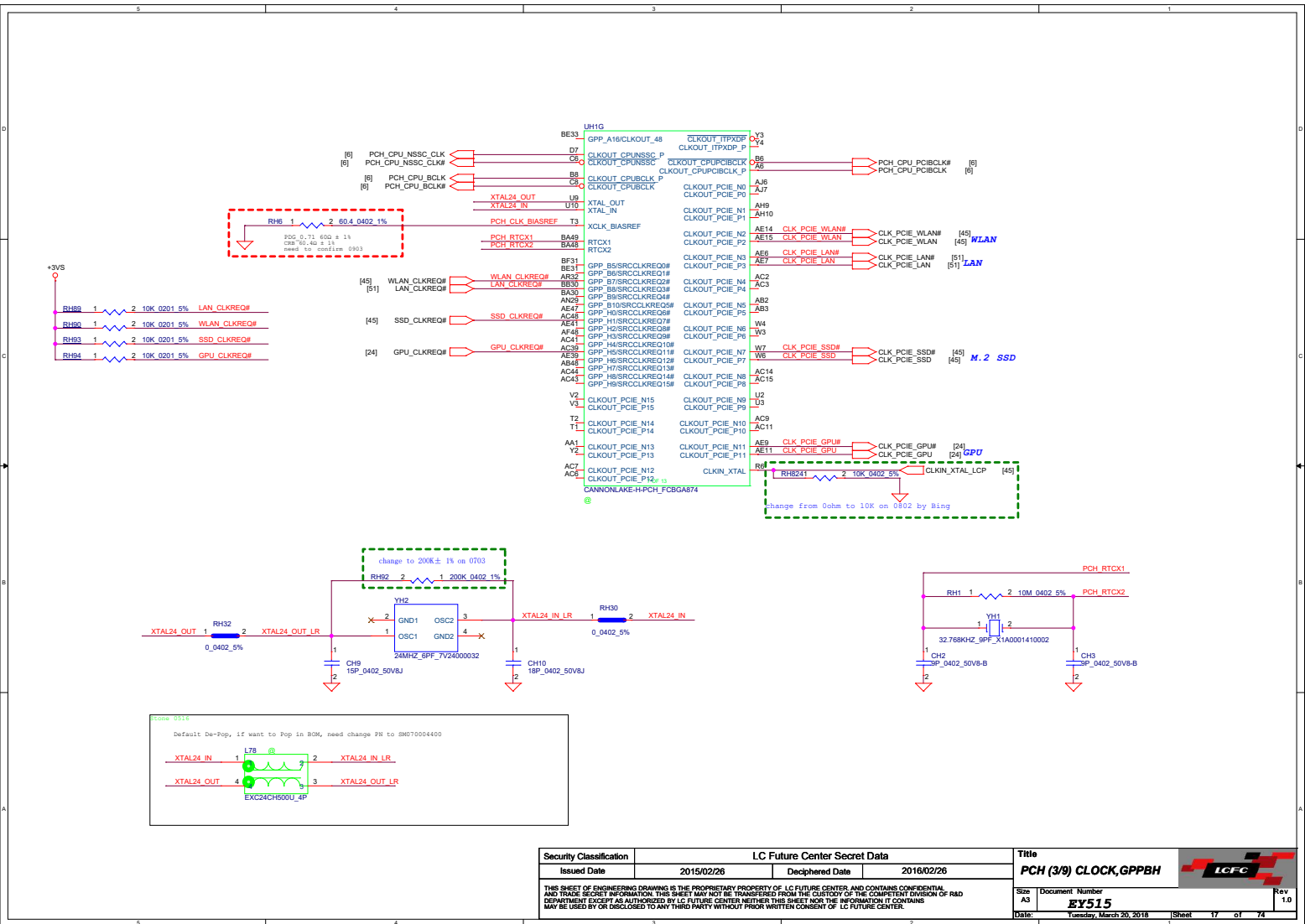


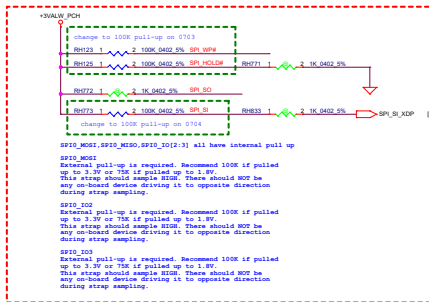
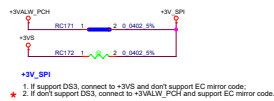
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/02/26	Deciphered Date	2016/02/26	PCH (1/9) PCIe/SATA/GPP/GP	
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				Date Tuesday, March 20, 2018	Sheet 14 of 24



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Issued Date	2015/02/26	Deciphered Date	2016/02/26	PCH (2/9) USB3/GPPAEFGHI			
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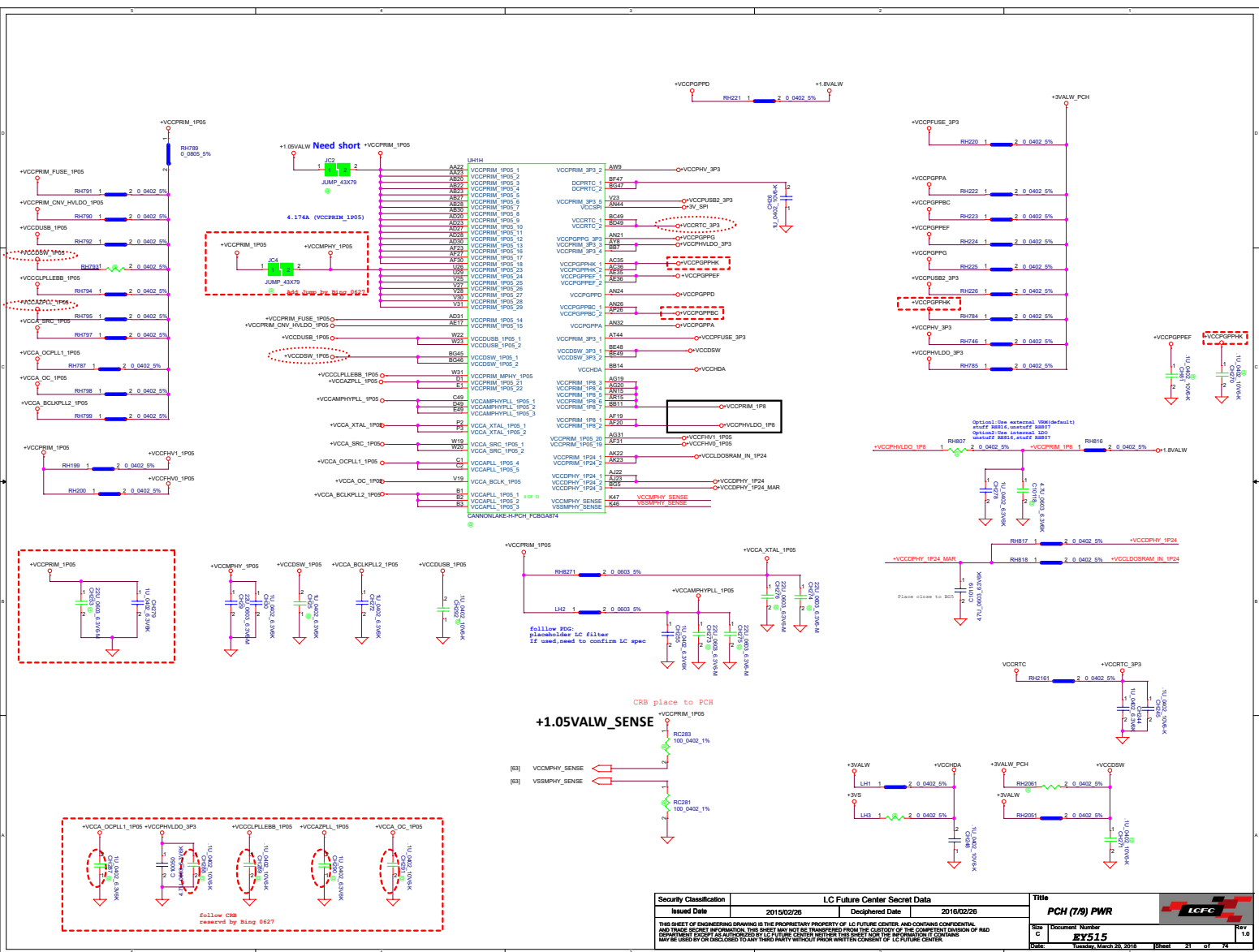
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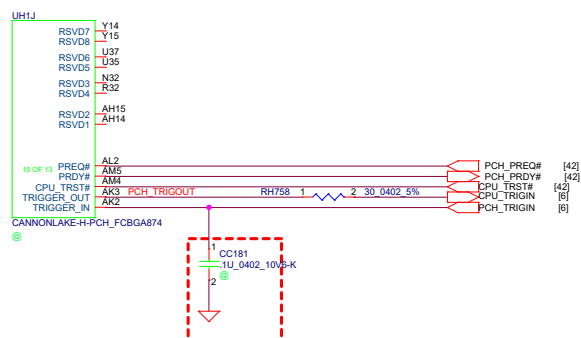
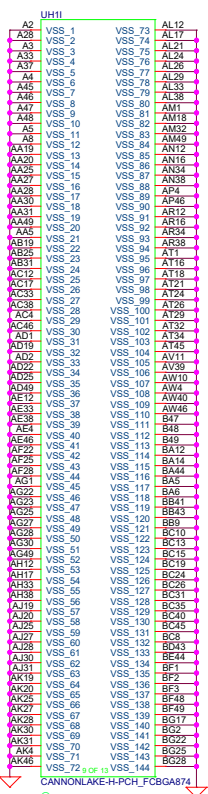
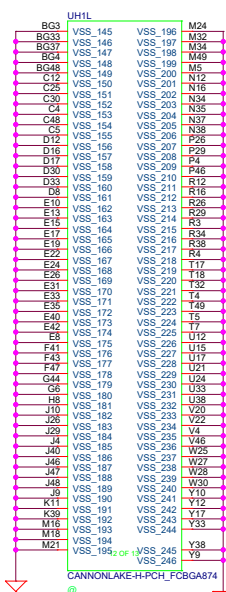
GPP_RIS/DBGALARMN (Strap reserved)
Strap pull-up is required. Second 100K if pulled
up to 3.3V or 75K if pulled up to 1.8V.
The strap should be disabled to operate.
Warning: This strap should be disabled. There should NOT be
any on-board device driving it in opposite direction
during strap sampling.
Power/Fuse: Primary Well

GPP_RIS/DBGALARMN
This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled
(Default)
1 = Master Attached Flash Sharing (MAFS) enabled.
Warning: This strap must be configured to ' 0 '
(MAFS is disabled) if the sSP of sPC
strap is configured to ' 0 ' (sSP
is disabled)
Notes:
1. The internal pull-down is disabled after ROMWRT
de-assertion.
2. This signal is in the primary well.

```

Security Classification	LC Future Center Secret Data		Title
Issued Date	2016/02/26	Declassified Date	PCH (S) SPI,SMBUS,GPPBEG
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Size A	Document Number	Rev	Rev
A	EVS15	00	1.0





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Issued Date	2015/02/26	Deciphered Date	2016/02/26
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Title	<i>PCH (9/9) VSS</i>
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Size B	Document Number EY515
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Date: Tuesday, March 10, 2009



Rev
1.0

N17P-G1 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU wake signal for GC6 2.1	
GPIO3	OUT	-	PWM Output to control the SRAM power supply	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control (100K pull Down)	
GPIO11	OUT	-	Panel Power enable	
GPIO12	IN	-	AC power detect or power supply overdraw input (10K pull High)	
GPIO13	OUT	N/A	LCD Panel Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA	
GPIO15	IN	N/A	Hot Plug Detect for IFPB	
GPIO16	OUT	-	System side PCIe reset monitor	
GPIO17	IN	N/A	Hot Plug Detect for IFPD	
GPIO18	IN	N/A	Hot Plug Detect for IFPE	
GPIO19	OUT	N/A	3D Vision L/R Signal	
GPIO20	N/A	N/A	GC5_MODE	
GPIO21	I/O	N/A	UNUSED	
GPIO22	I/O	N/A	UNUSED	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24	IN	N/A	Hot Plug Detect for IFPF	
GPIO25		N/A	UNUSED	
GPIO26		N/A	UNUSED	
GPIO27	IN	N/A	Hot Plug Detect for IFPC	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

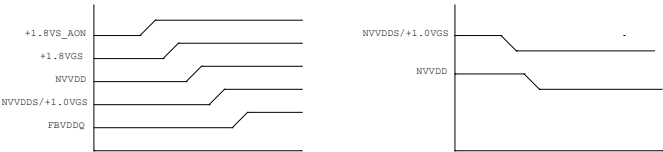
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1=ENABLE 0=DISABLE
SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCIIE_CFG LOW POWER
0:PCIIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

N17P-G1 Power Sequence



1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.

2. V (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Pgood) must NOT exceed 80V.

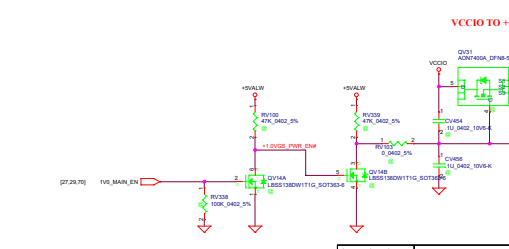
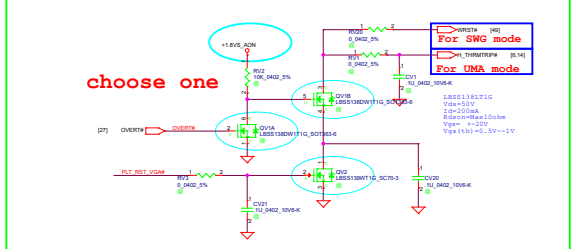
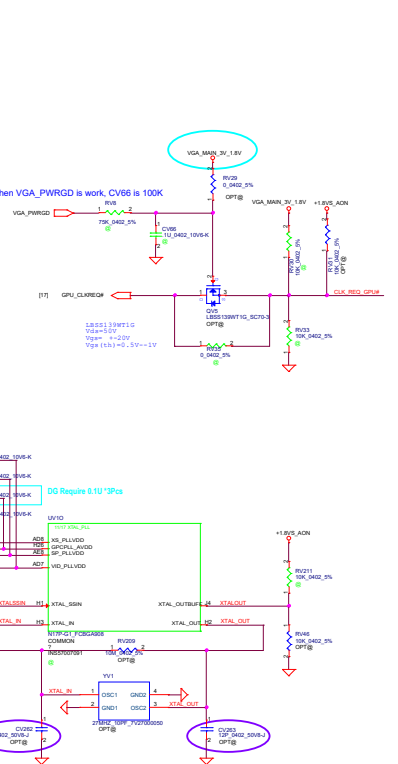
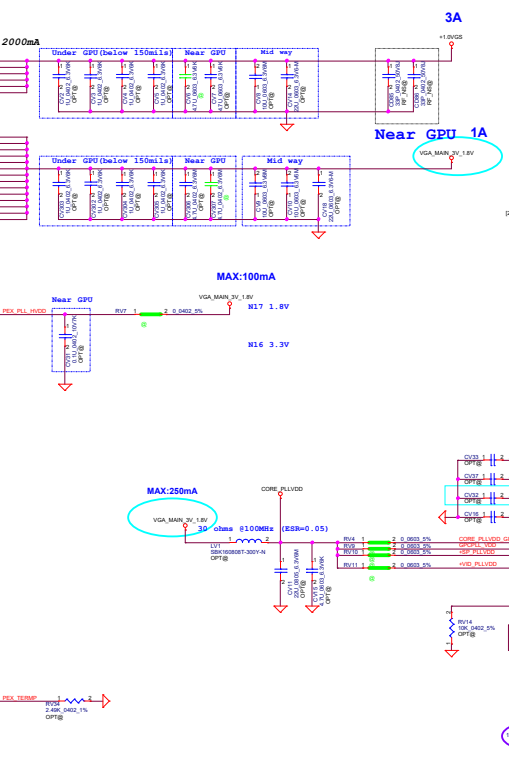
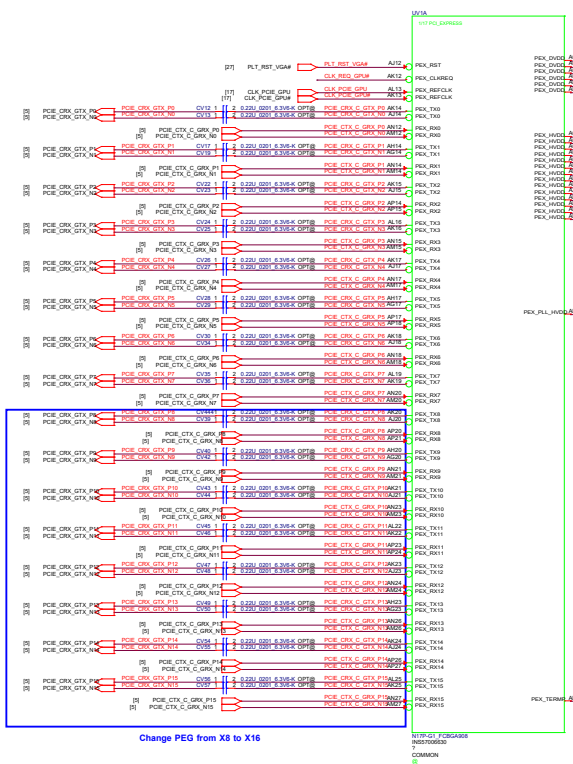
3. All 3.3V devices that connect to the GPU must be powered after 1V8_AON. GPU can NOT have any 3.3V leakage path before 1V8_AON present.

4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.
1. NVVDDSD/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.

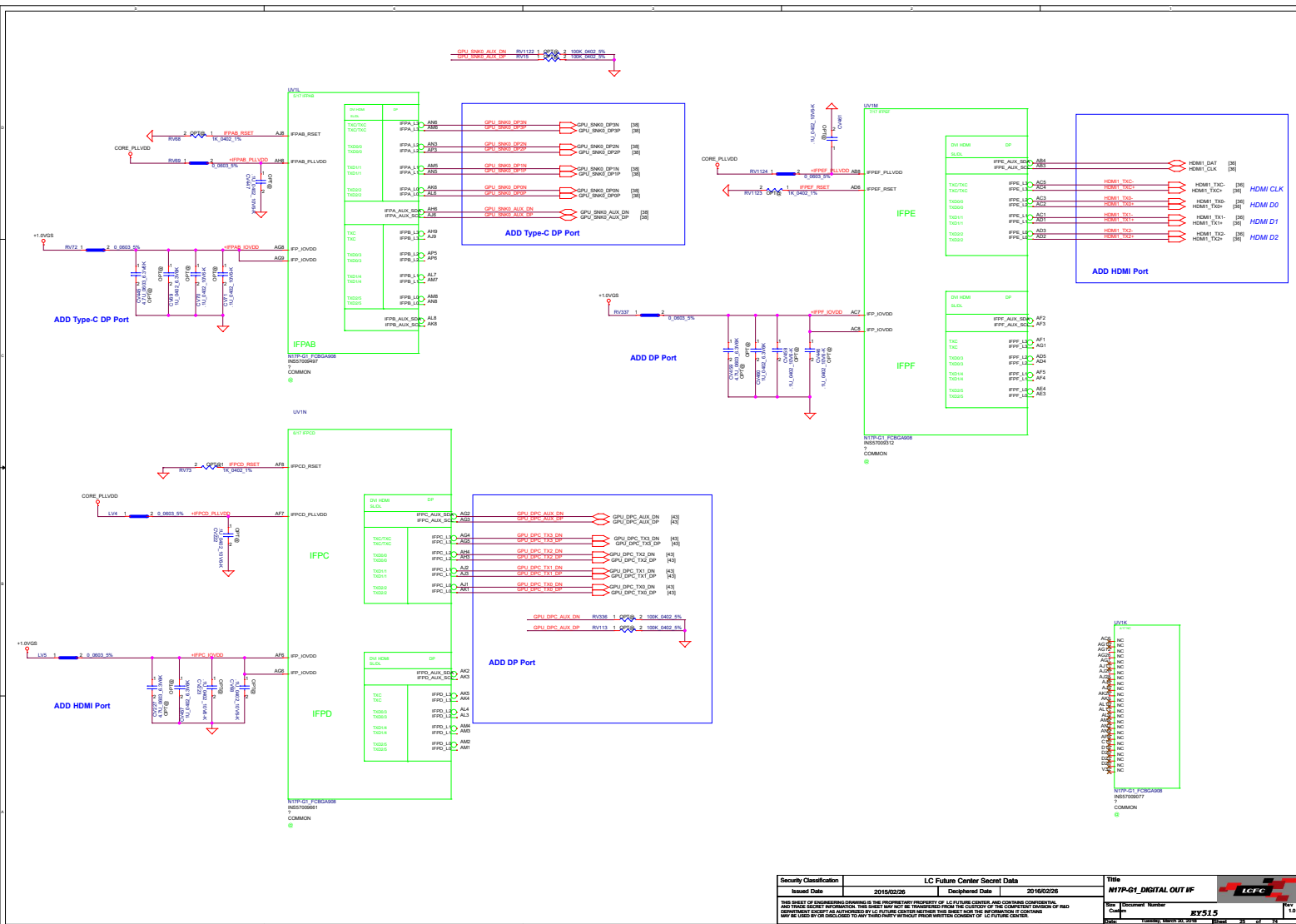
2. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON. GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

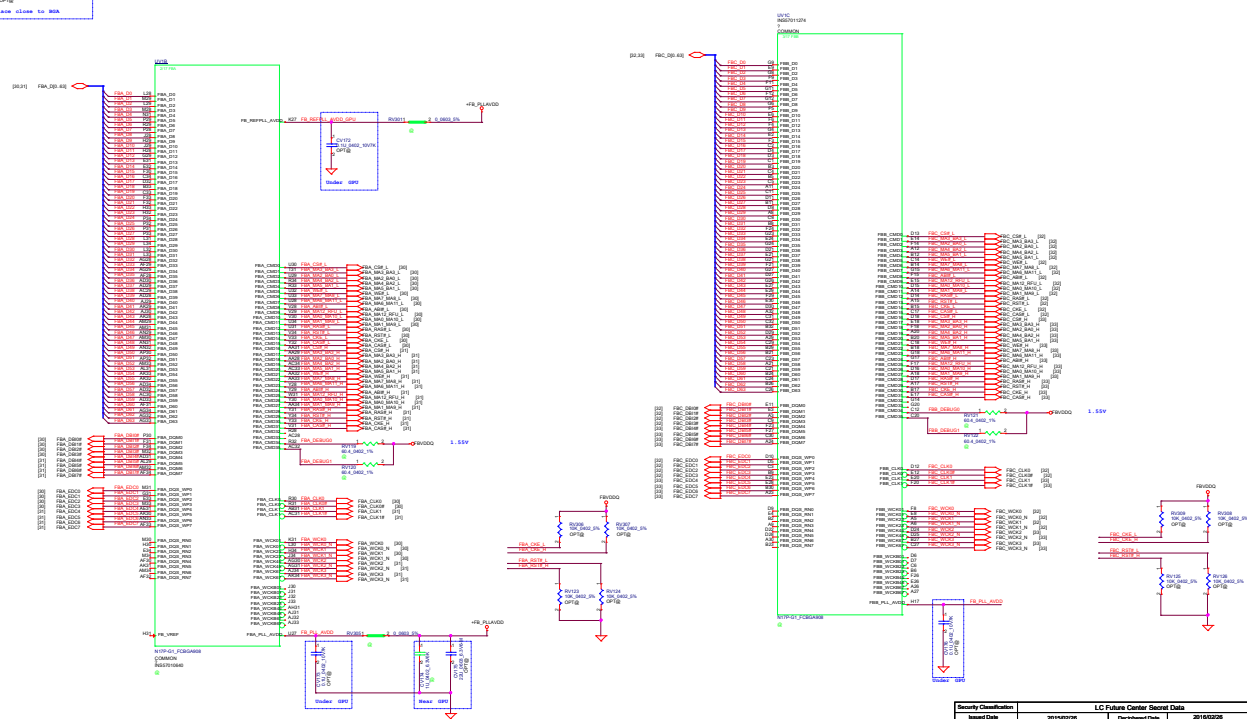
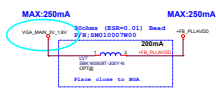
3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

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		2016/02/28		VGA Notes List	
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Rev C		Document Number		EVS15	
VDATE		Tuesday, March 20, 2015		Printed 23 of 24	



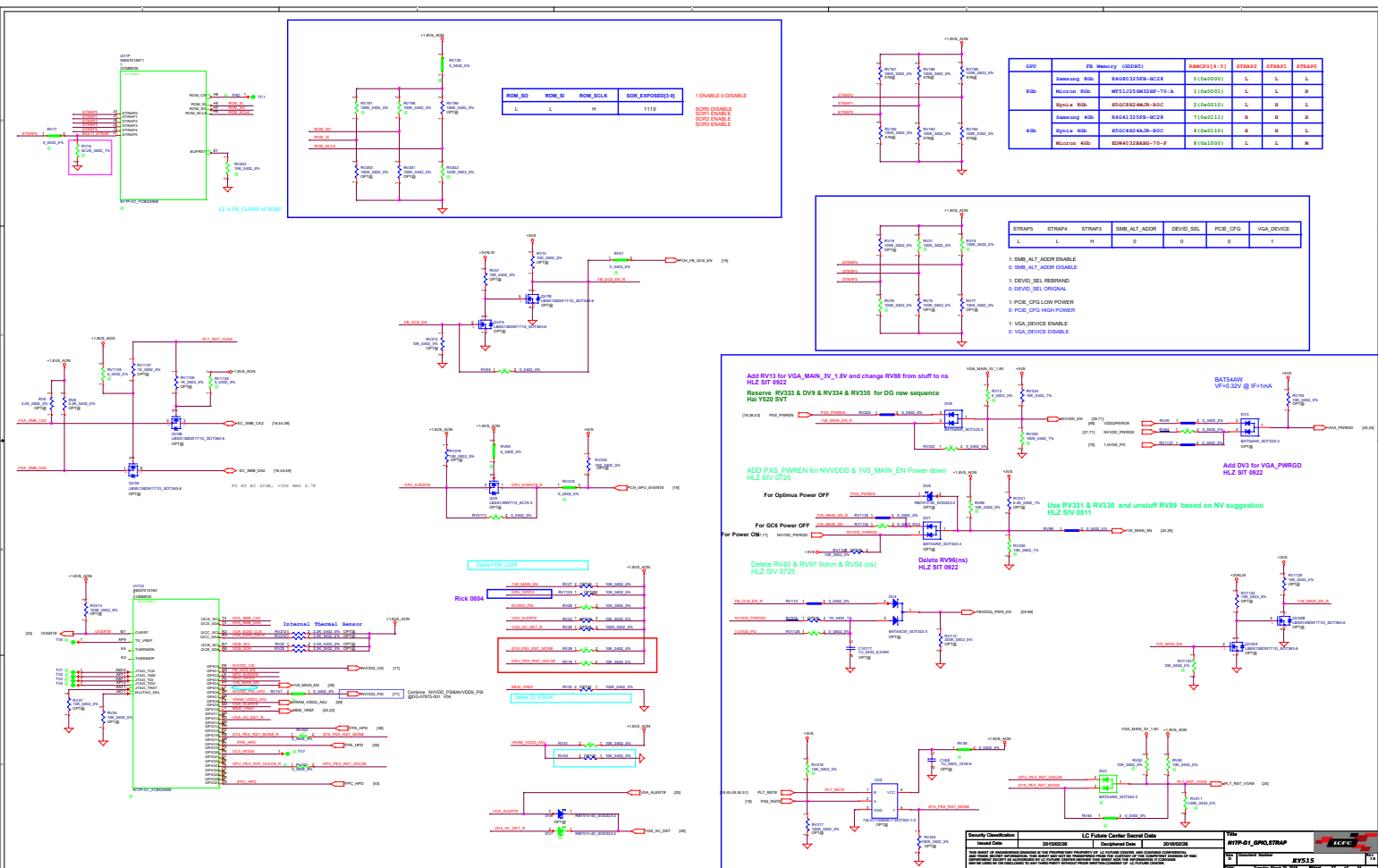
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/02/28	Declassified Date	2016/02/28	N77-G1_PEG IF	
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Approved For Release		Declassified		N77-G1_PEG IF	



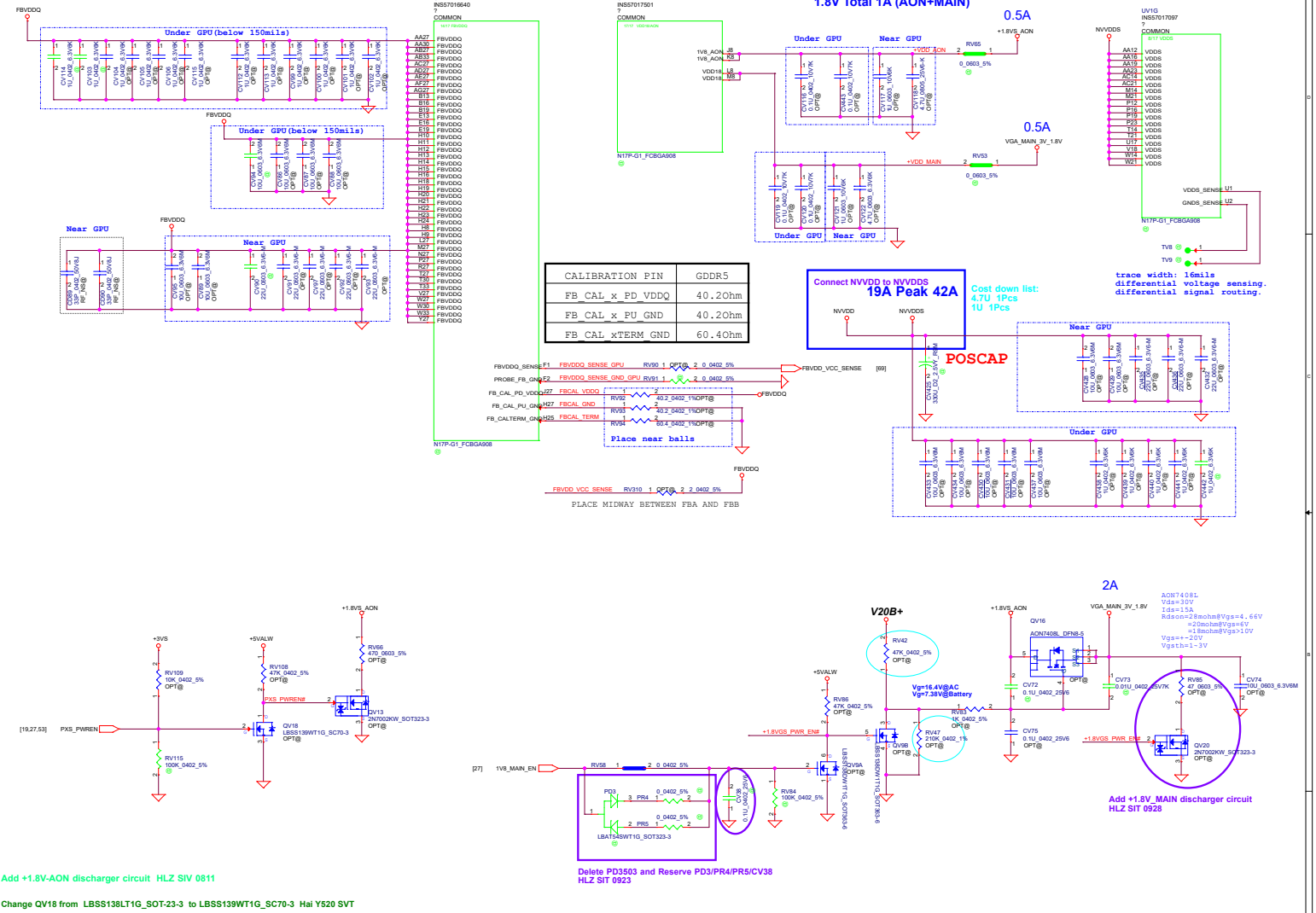


GD085
Mode II - Mirror Mode Mapping

DATA Size	
0x00	0x00
0x01	0x01
0x02	0x02
0x03	0x03
0x04	0x04
0x05	0x05
0x06	0x06
0x07	0x07
0x08	0x08
0x09	0x09
0x0A	0x0A
0x0B	0x0B
0x0C	0x0C
0x0D	0x0D
0x0E	0x0E
0x0F	0x0F
0x10	0x10
0x11	0x11
0x12	0x12
0x13	0x13
0x14	0x14
0x15	0x15
0x16	0x16
0x17	0x17
0x18	0x18
0x19	0x19
0x1A	0x1A
0x1B	0x1B
0x1C	0x1C
0x1D	0x1D
0x1E	0x1E
0x1F	0x1F
0x20	0x20
0x21	0x21
0x22	0x22
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0x24	0x24
0x25	0x25
0x26	0x26
0x27	0x27
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0x29	0x29
0x2A	0x2A
0x2B	0x2B
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0x2D	0x2D
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0x9B	0x9B
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0x9E	0x9E
0x9F	0x9F
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0xA6	0xA6
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0xAF	0xAF
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0xB1	0xB1
0xB2	0xB2
0xB3	0xB3
0xB4	0xB4
0xB5	0xB5
0xB6	0xB6
0xB7	0xB7
0xB8	0xB8
0xB9	0xB9
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0xBF	0xBF
0xC0	0xC0
0xC1	0xC1
0xC2	0xC2
0xC3	0xC3
0xC4	0xC4
0xC5	0xC5
0xC6	0xC6
0xC7	0xC7
0xC8	0xC8
0xC9	0xC9
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0xCB	0xCB
0xCC	0xCC
0xCD	0xCD
0xCE	0xCE
0xCF	0xCF
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0xD2	0xD2
0xD3	0xD3
0xD4	0xD4
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0xD6	0xD6
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0xD8	0xD8
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0xFF	0xFF



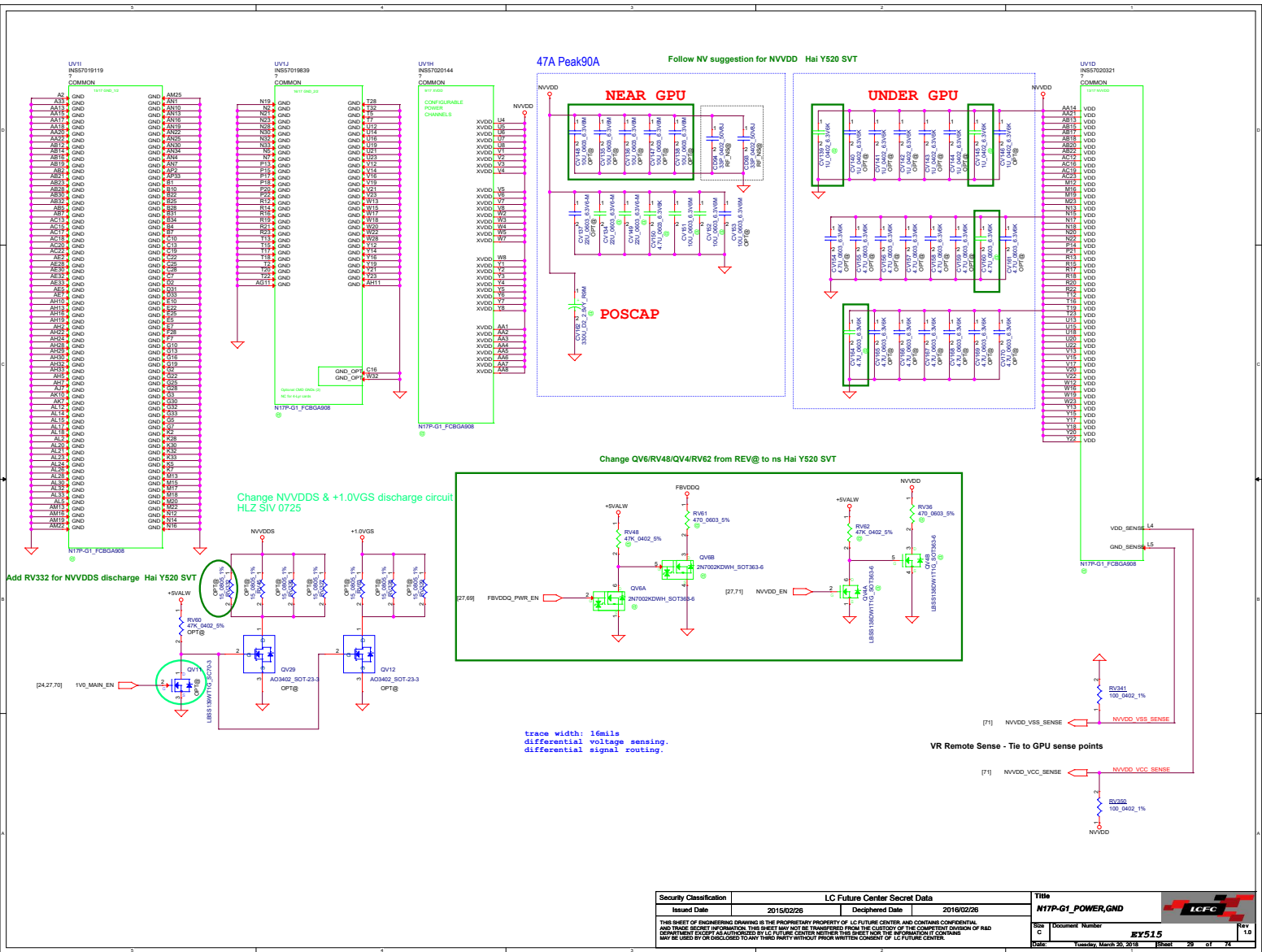
5A Peak 8A



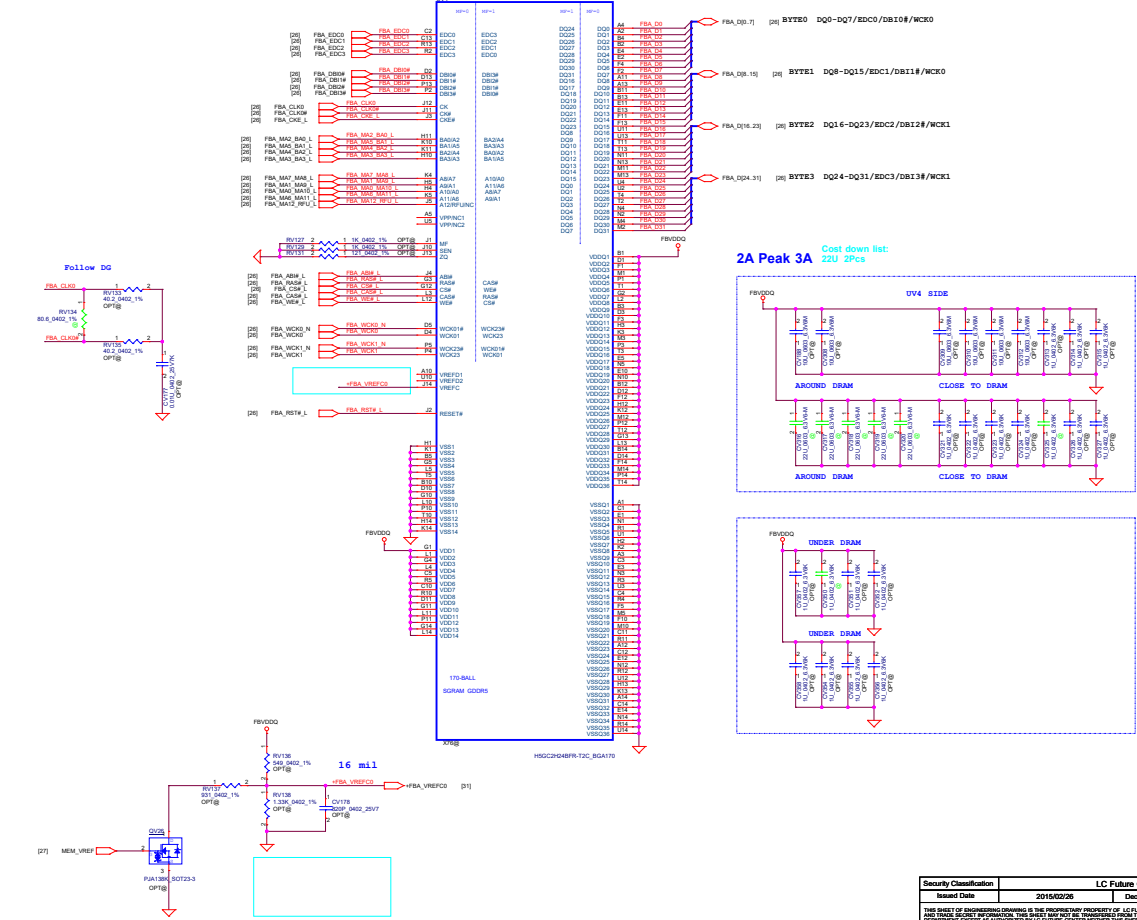
Add +1.8V-AON discharger circuit. HLZ SIV 0811

Change QV18 from LBSS138LT1G_SOT-23-3 to LBSS139WT1G_SC70-3 Hai Y520 SVT

Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		N17P-G1_POWER	
2015/02/28		2016/02/28			
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Rev	Document Number	EY515		Rev	
1.0					
Date		Version		Sheet	
March 20, 2016				28 of 34	



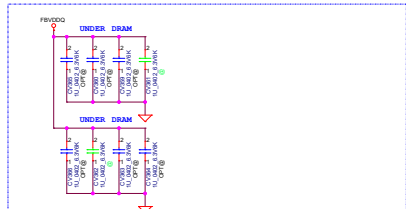
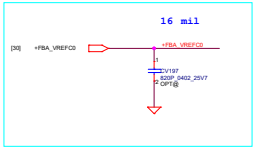
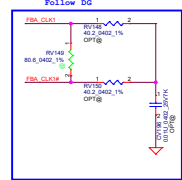
Memory Partition A - Lower 64 bits (MF=0)



GDDR5 Mode H - Mirror Mode Mapping

Address	DATA Bus
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FBx_CHD1	A3_BA0
FBx_CHD2	A4_BA2
FBx_CHD3	A4_BA1
FBx_CHD4	A7_A8
FBx_CHD5	A8_A11
FBx_CHD6	A8_A11
FBx_CHD7	A8_A11
FBx_CHD8	A8_A11
FBx_CHD9	A8_A11
FBx_CHD10	A8_A11
FBx_CHD11	A8_A11
FBx_CHD12	A8_A11
FBx_CHD13	A8_A11
FBx_CHD14	A8_A11
FBx_CHD15	A8_A11
FBx_CHD16	A8_A11
FBx_CHD17	A8_A11
FBx_CHD18	A8_A11
FBx_CHD19	A8_A11
FBx_CHD20	A8_A11
FBx_CHD21	A8_A11
FBx_CHD22	A8_A11
FBx_CHD23	A8_A11
FBx_CHD24	A8_A11
FBx_CHD25	A8_A11
FBx_CHD26	A8_A11
FBx_CHD27	A8_A11
FBx_CHD28	A8_A11
FBx_CHD29	A8_A11
FBx_CHD30	A8_A11
FBx_CHD31	A8_A11

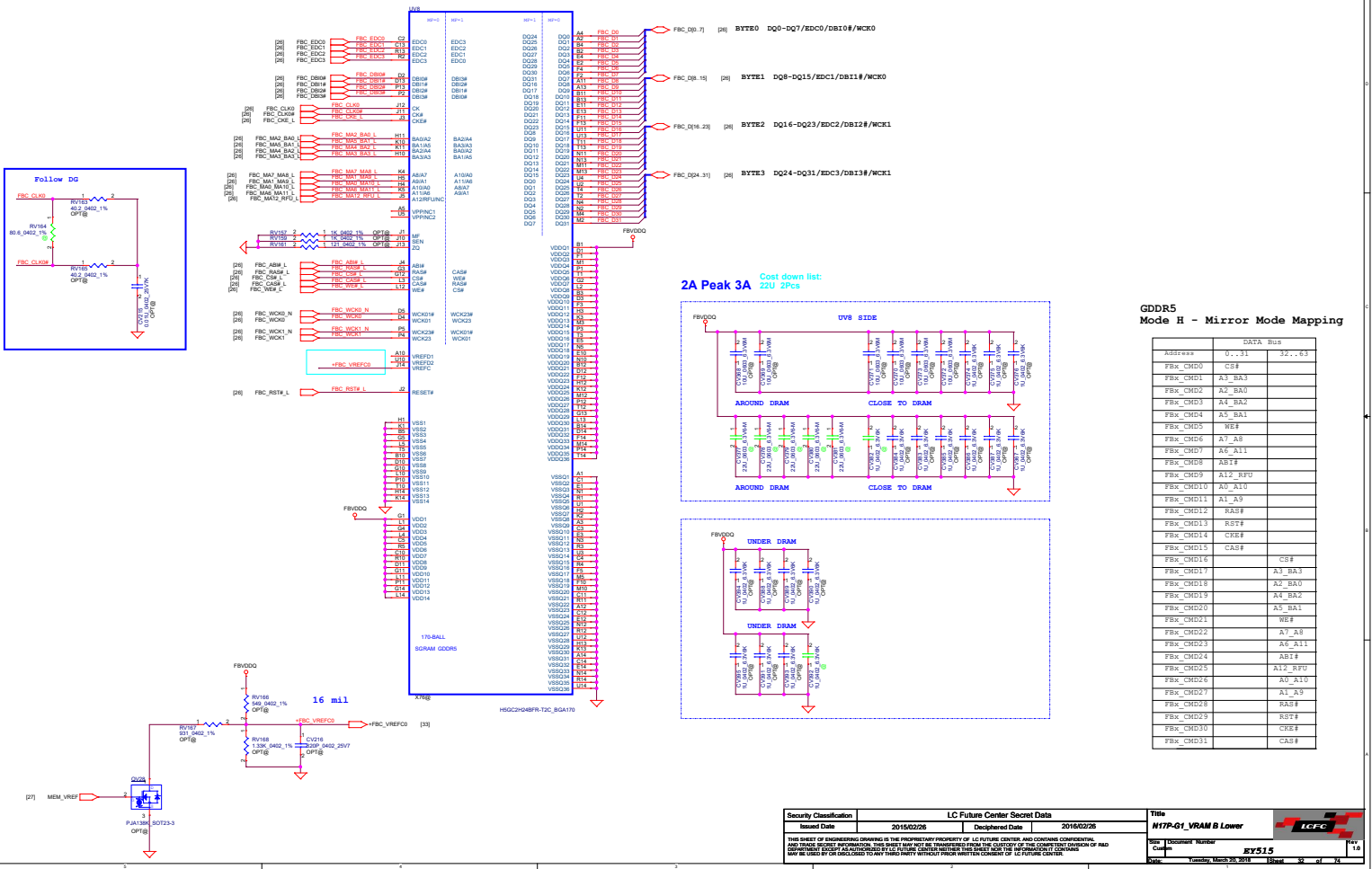
Memory Partition A- Upper 64 bits (MF=0)



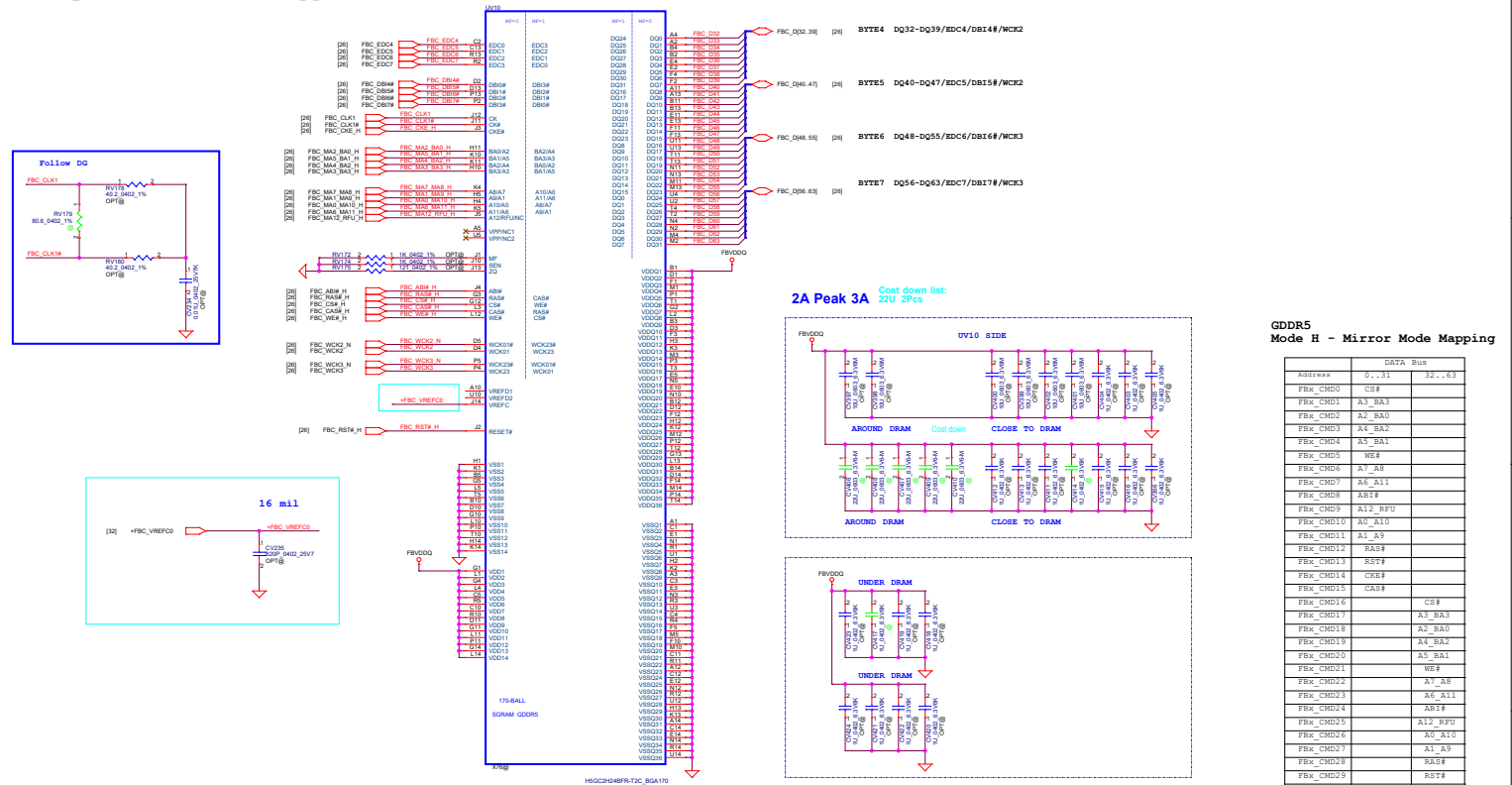
GDDR5
Mode H - Mirror Mode Mapping

Address	DATA BUS	
	0...31	32...63
FRX_DMG0	CSF	
FRX_DMG1	A1_BA1	
FRX_DMG2	A2_BA2	
FRX_DMG3	A3_BA3	
FRX_DMG4	A4_BA4	
FRX_DMG5	HEF	
FRX_DMG6	A1_A3	
FRX_DMG7	A4_A12	
FRX_DMG8	ABT4	
FRX_DMG9	A12_RFD	
FRX_DMG10	A0_A10	
FRX_DMG11	A1_A9	
FRX_DMG12	CSF4	
FRX_DMG13	RS74	
FRX_DMG14	CRS4	
FRX_DMG15	CSF4	
FRX_DMG16		CSF
FRX_DMG17		A3_BA3
FRX_DMG18		A2_BA2
FRX_DMG19		A4_BA4
FRX_DMG20		A3_BA3
FRX_DMG21		HEF
FRX_DMG22		A1_A3
FRX_DMG23		A12_RFD
FRX_DMG24		ABT4
FRX_DMG25		A12_RFD
FRX_DMG26		A1_A9
FRX_DMG27		RS74
FRX_DMG28		CRS4
FRX_DMG29		CSF4
FRX_DMG30		CSF
FRX_DMG31		CSF4

Memory Partition B - Lower 32 bits(MF=0)

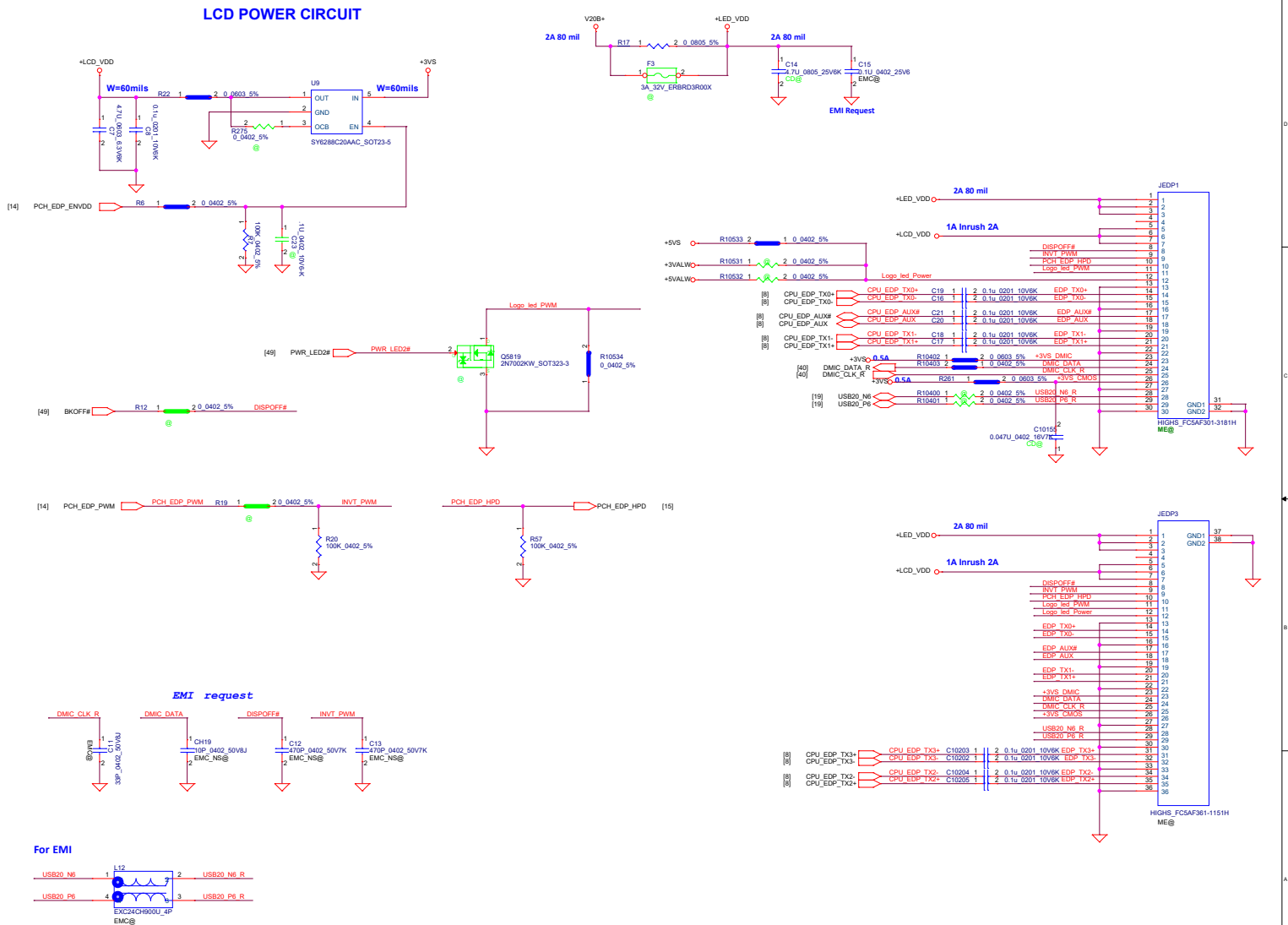



Memory Partition B - Upper 32 bits (MF=0)

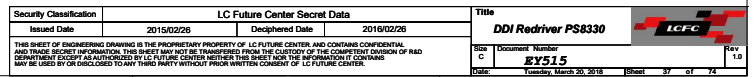


MODE5		
Mode B - Mirror Mode Mapping		
Address	DATA Bus	
FXB_C0D0	CS#	32...C03
FXB_C0D1	A1..BA3	
FXB_C0D2	A2..BA0	
FXB_C0D3	A1..BA2	
FXB_C0D4	A5..BA1	
FXB_C0D5	WE#	
FXB_C0D6	A7..A6	
FXB_C0D7	A6..A11	
FXB_C0D8	AB1#	
FXB_C0D9	A12..RPU	
FXB_C0D10	A0..A10	
FXB_C0D11	A1..A9	
FXB_C0D12	RST#	
FXB_C0D13	RST#	
FXB_C0D14	CKE#	
FXB_C0D15	CA#	
FXB_C0D16	CS#	
FXB_C0D17	A3..BA1	
FXB_C0D18	A2..BA0	
FXB_C0D19	A3..BA1	
FXB_C0D20	A2..BA1	
FXB_C0D21	WE#	
FXB_C0D22	A7..A6	
FXB_C0D23	A6..A11	
FXB_C0D24	AB1#	
FXB_C0D25	A12..RPU	
FXB_C0D26	A0..A10	
FXB_C0D27	A1..A9	
FXB_C0D28	RST#	
FXB_C0D29	RST#	
FXB_C0D30	CKE#	
FXB_C0D31	CA#	

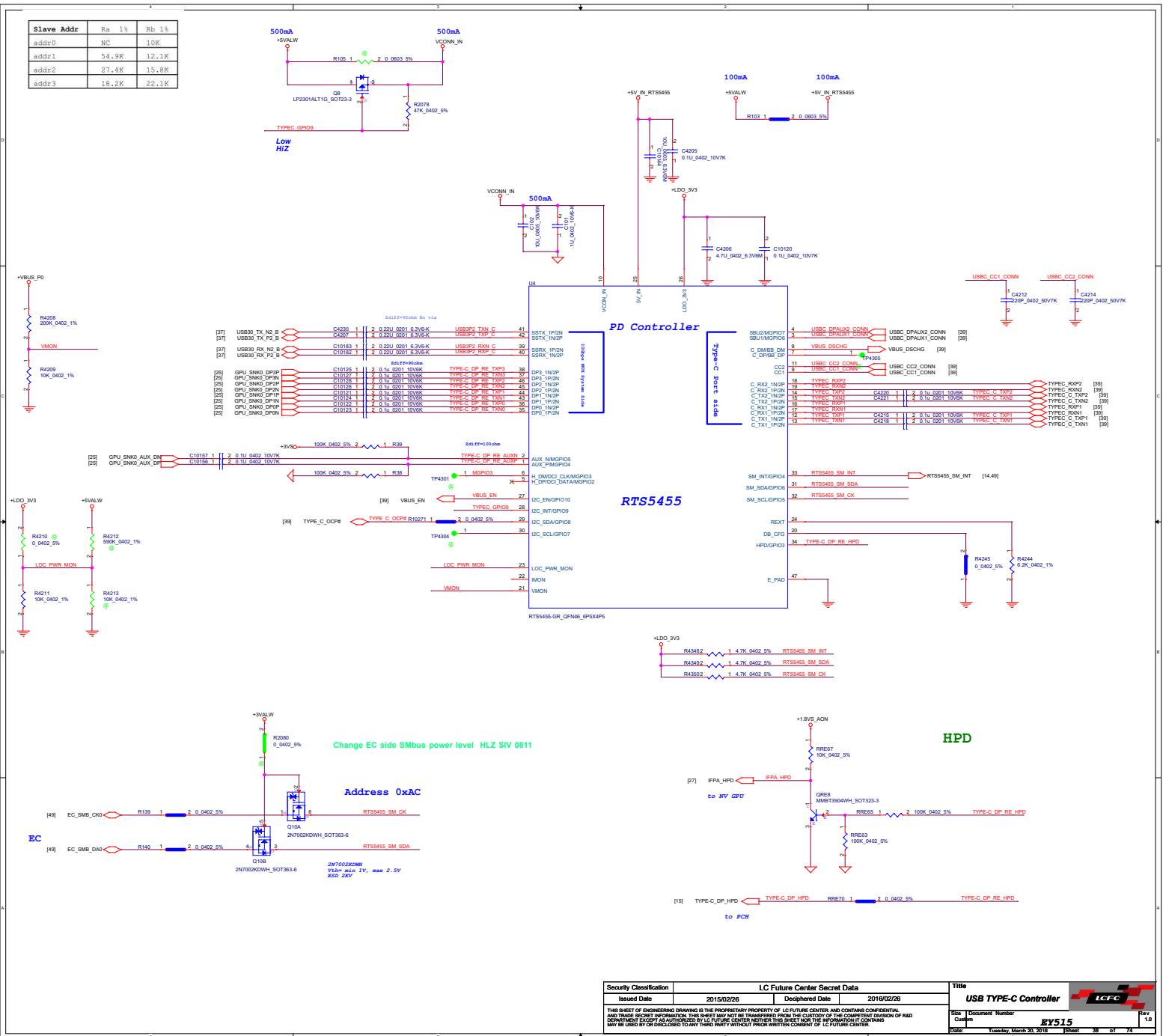
LCD POWER CIRCUIT



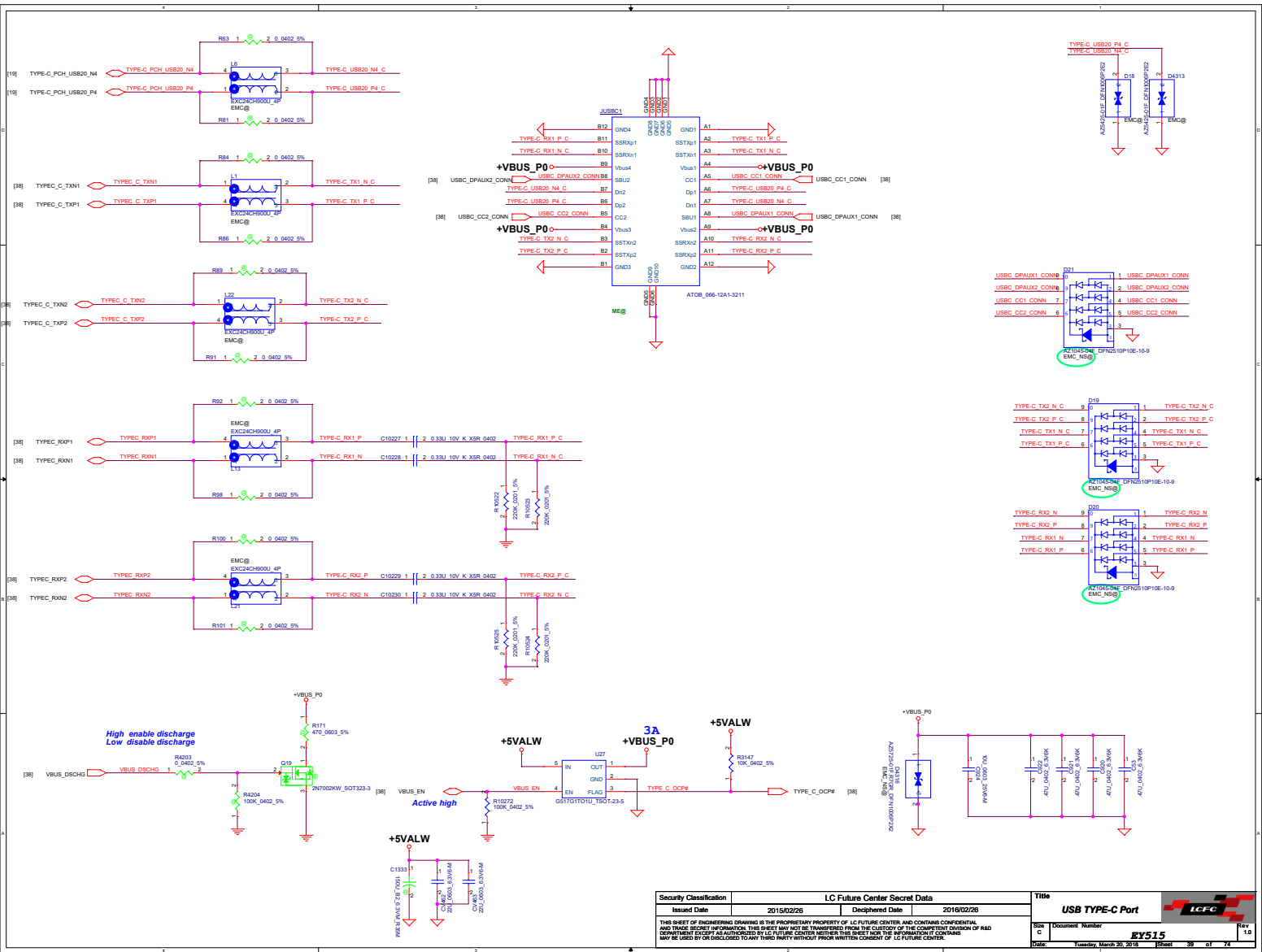
Security Classification	LC Future Center Secret Data			Title		
Issued Date	2015/02/26	Deciphered Date	2016/02/26	eDP/CMOS/Touch screen		
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				Size	Document Number	Rev
				Date	EY515	1.0
				Created	Tuesday, March 20, 2016	Sheet 35 of 74




Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/02/26	Deciphered Date	2016/02/26	USB TYPE-C Controller	
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Rev	1.0	Document Number	EY515		
Date	Monday, March 20, 2016	Sheet	38	of	74

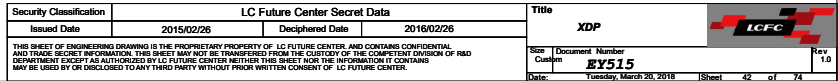


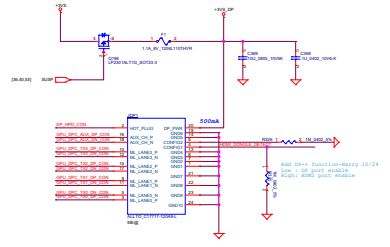
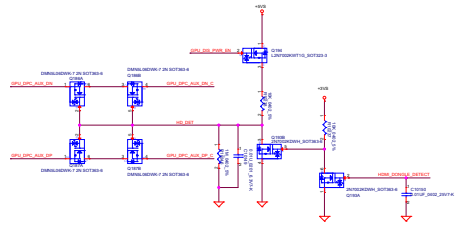
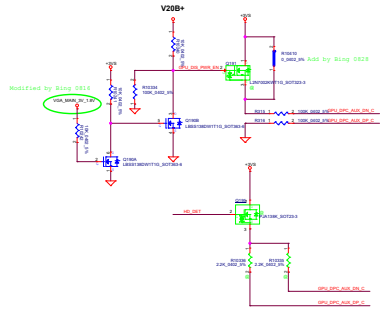
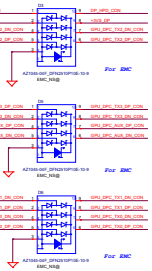
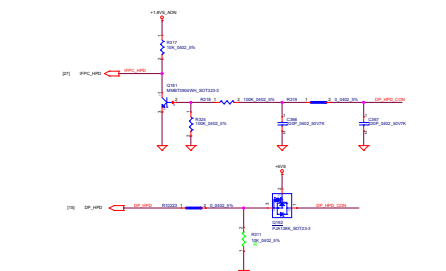
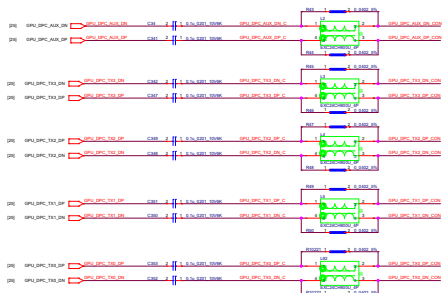


Security Classification	LC Future Center Secret Data		Title				
Issued Date	2015/6/23	Deciphered Date	2015/6/23		Audio Jack		
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				Date	Wednesday, March 20, 2018	Sheet	41 of 74

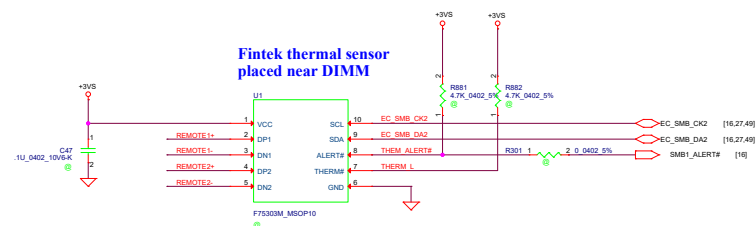
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R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

	No use	Individual Port	DC1 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

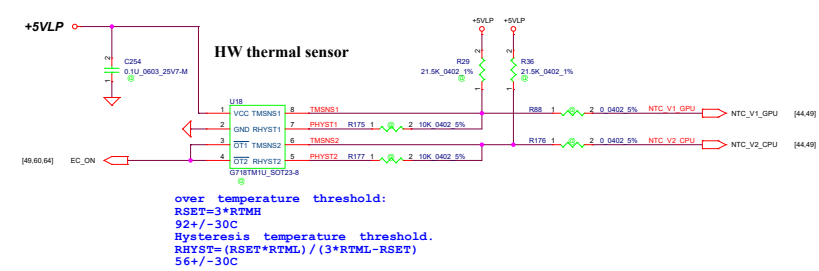
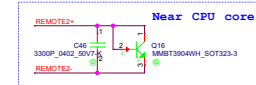
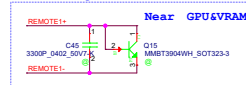




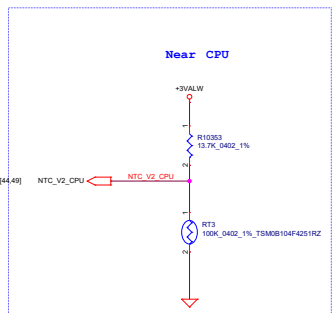
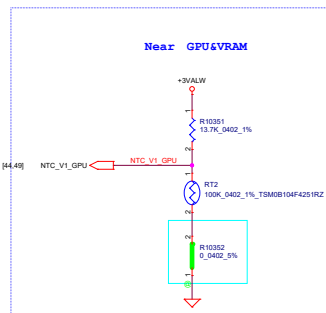
Security Classification		LC Future Center Secret Data		Title	
Secret Date	20130808	Declassify Date	20180808	DP	
Add GPU_Aux_Aux_DP_1 to GPU_Aux_Aux_DP_10					
Add GPU_Aux_Aux_DP_1 to GPU_Aux_Aux_DP_10					
Add GPU_Aux_Aux_DP_1 to GPU_Aux_Aux_DP_10					



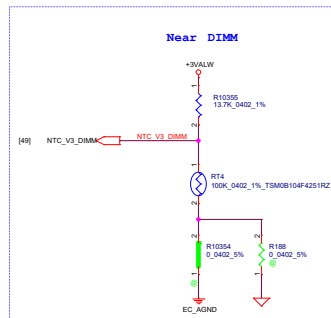
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

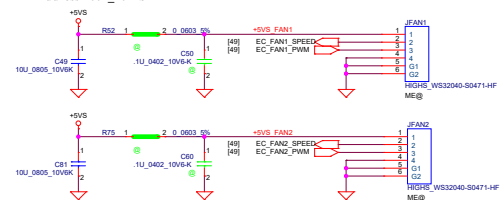


for layout optimized, change the EC_AGND to GND



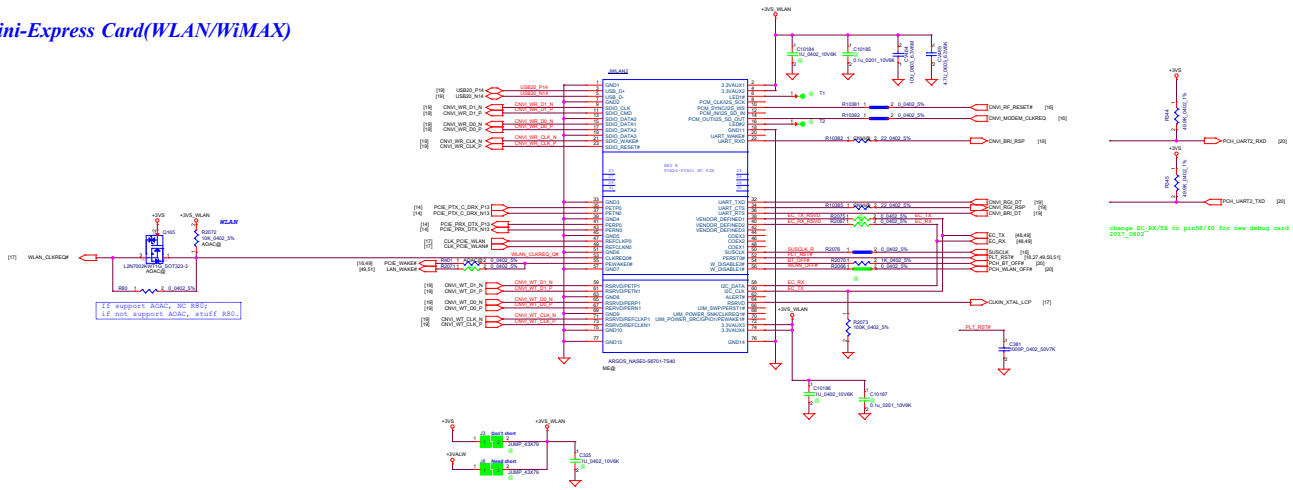
FAN Conn

Address 1001_101xb

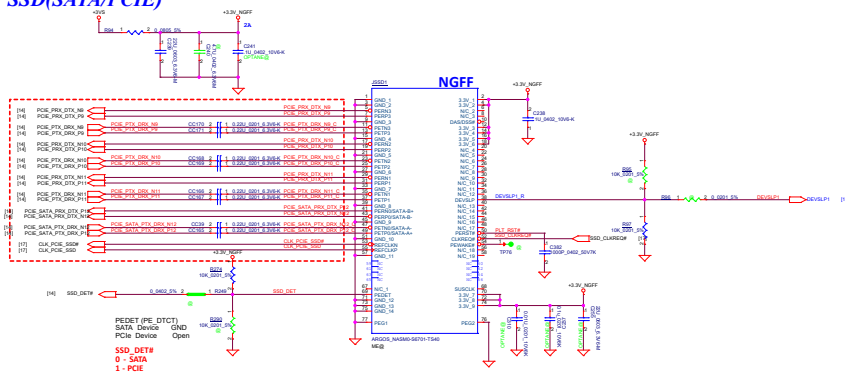


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/02/26	Deciphered Date	2016/02/26	Thermal sensor/FAN CONN	
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Rev	Document Number	Date		Sheet	
1.0	EV515	January 30th, 2015		44 of 74	

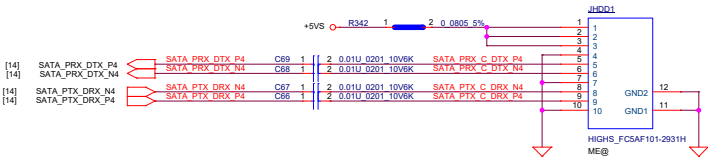
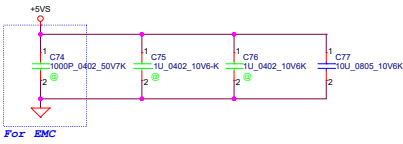
Mini-Express Card(WLAN/WiMAX)



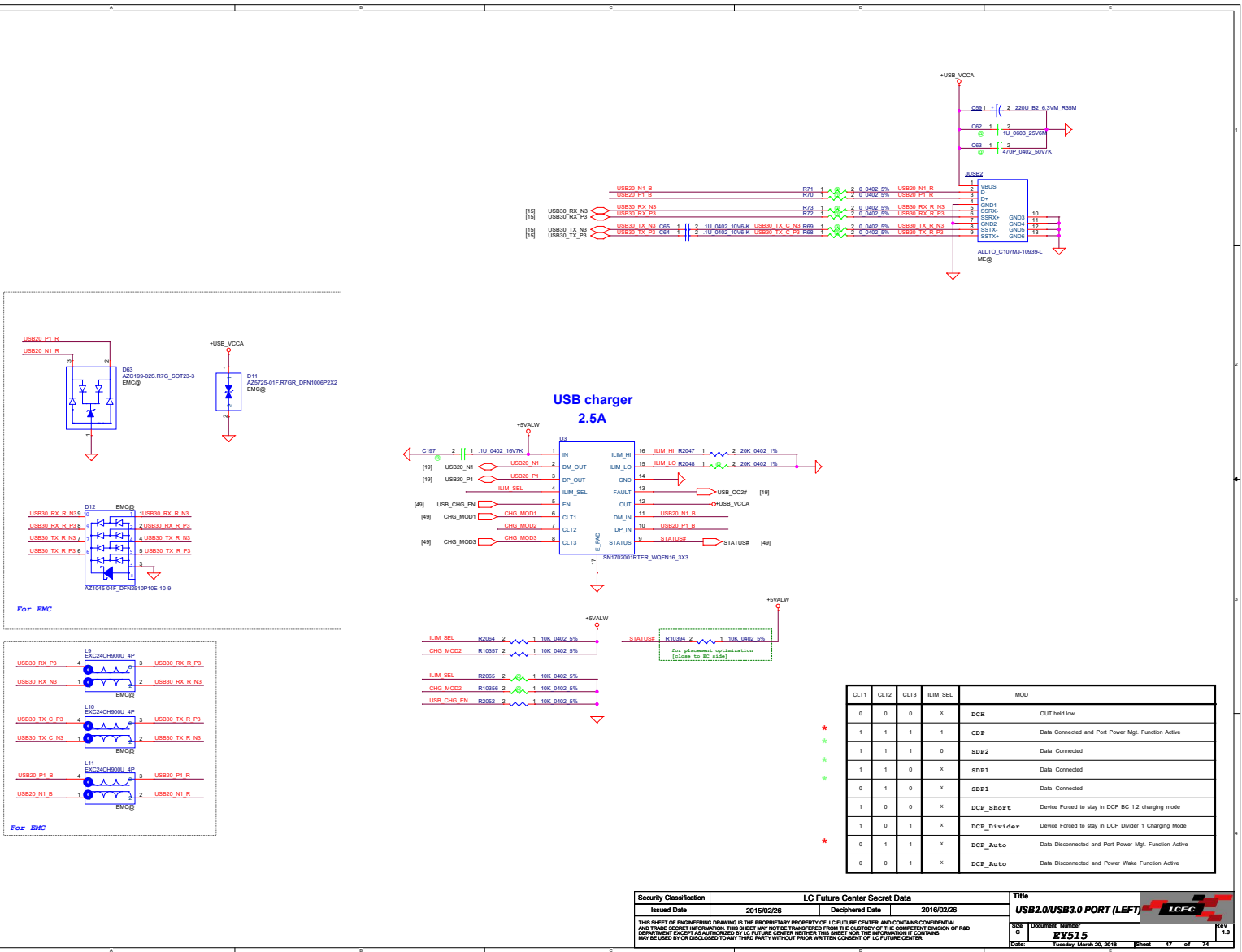
M.2 SSD(SATA/PCIE)

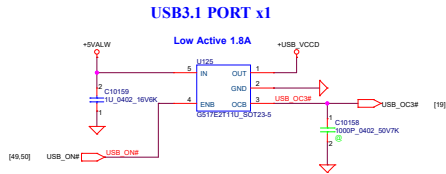
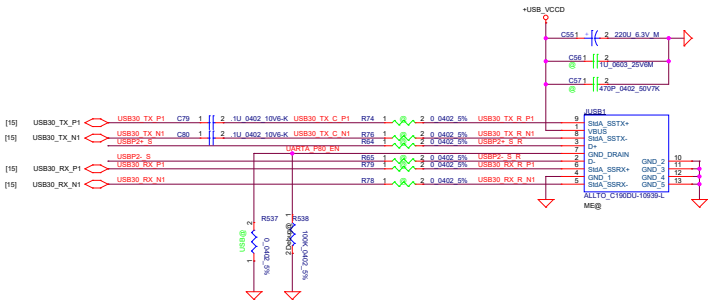


SATA HDD Conn.

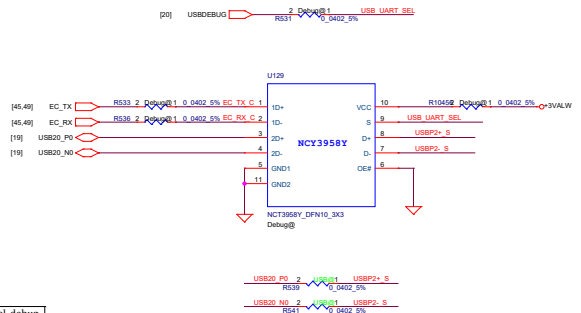
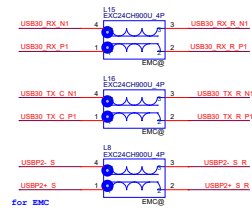
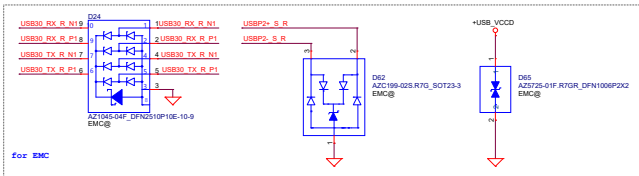


Security Classification	LC Future Center Secret Data			Title	HDD/XBOX CONN	
Issued Date	2015/02/26	Deciphered Date	2016/02/26	Size	Document Number	Rev
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				Date	Tuesday, March 20, 2016	Sheet 48 of 74





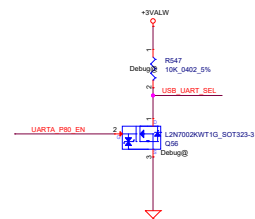
For USB Debug Function



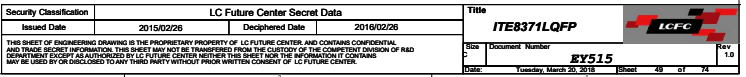
JSBDEBUG	Kernel debug
Set Logout	Set Logout
Set Logout Low	ENABLE

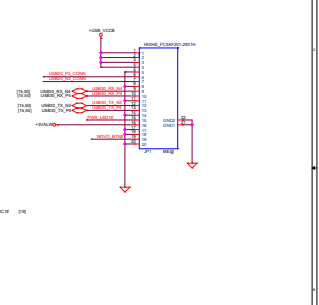
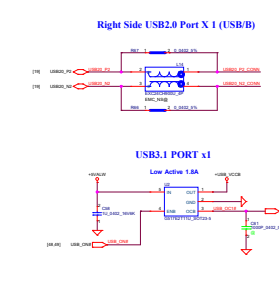
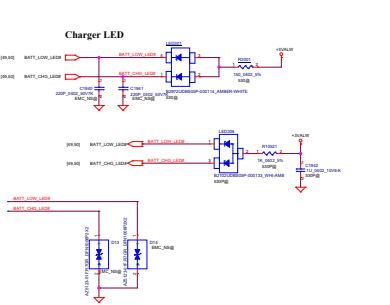
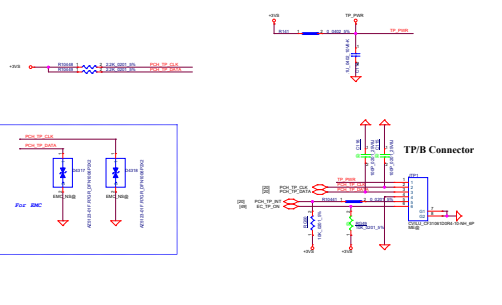
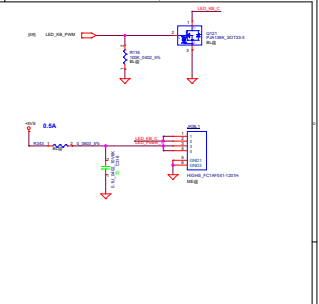
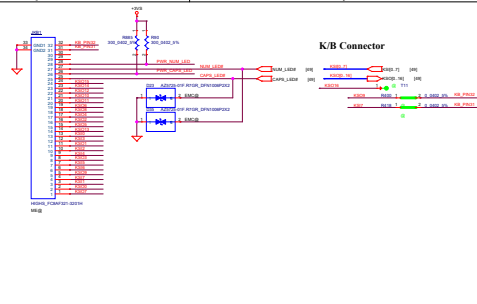
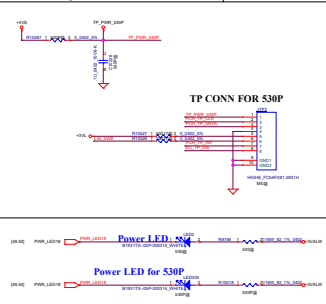
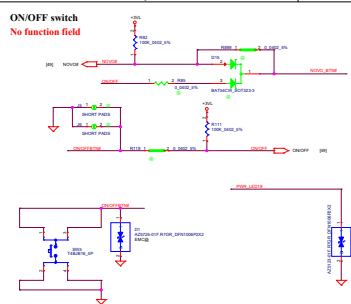
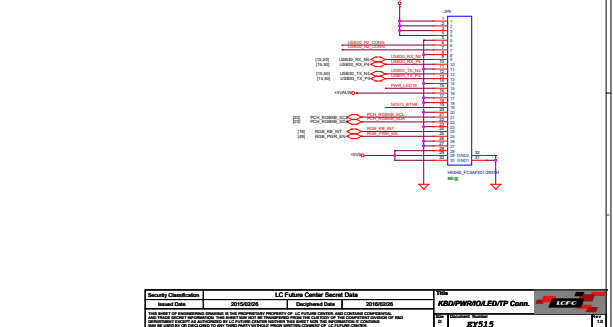
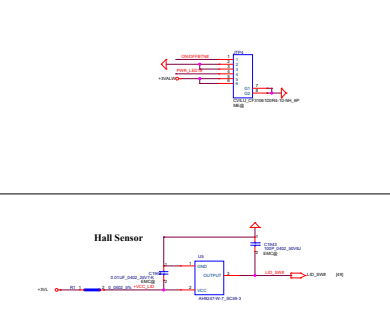
UARTA_P80_EN	POST 80
Set Logout	DISABLE
Set Logout Low	ENABLE

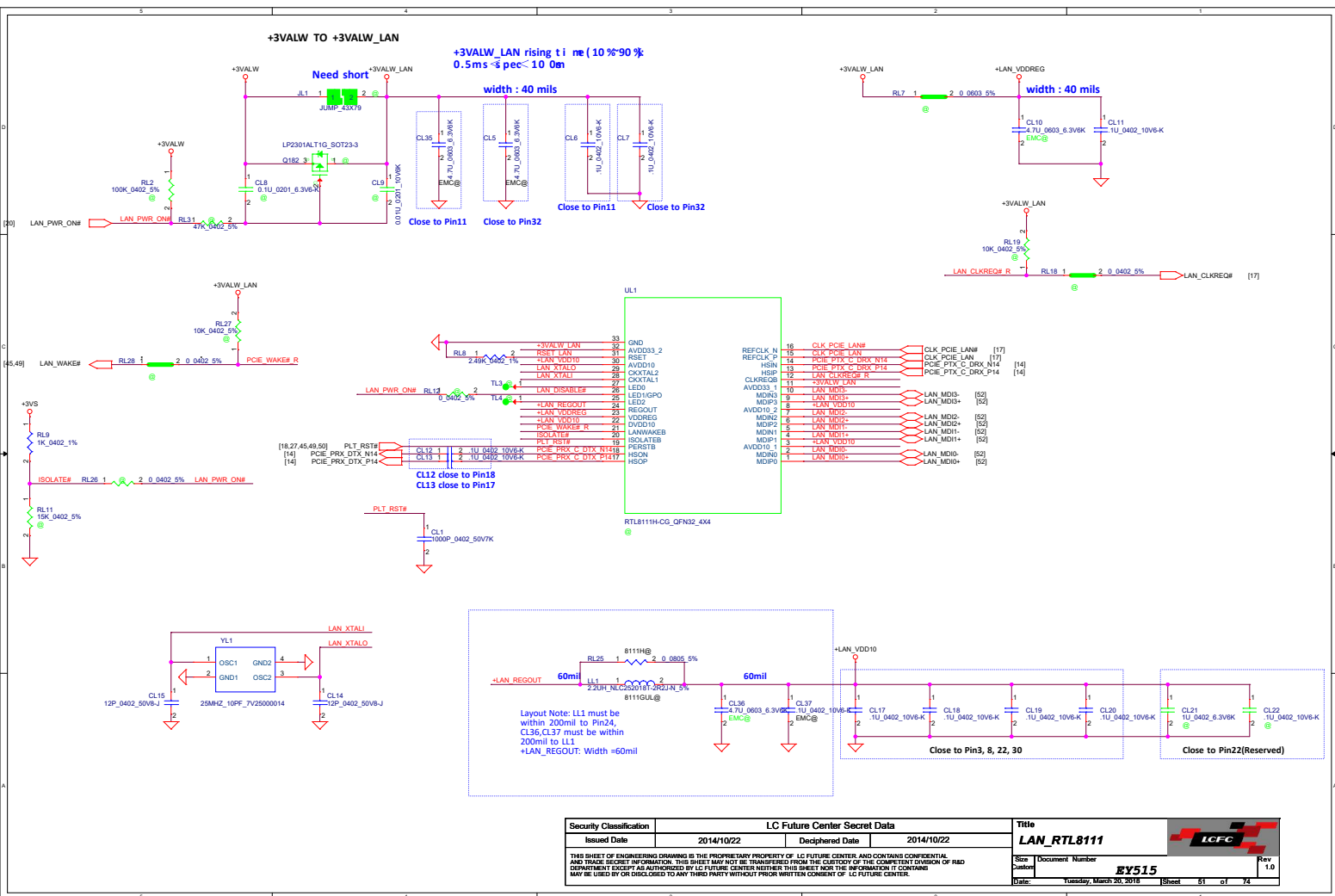
DE#	S	FUNCTION
0	X	DISABLE
1	L	2(n+/-) to 2D(n+/-)
2	R	2(n+/-) to 2D(n+/-)



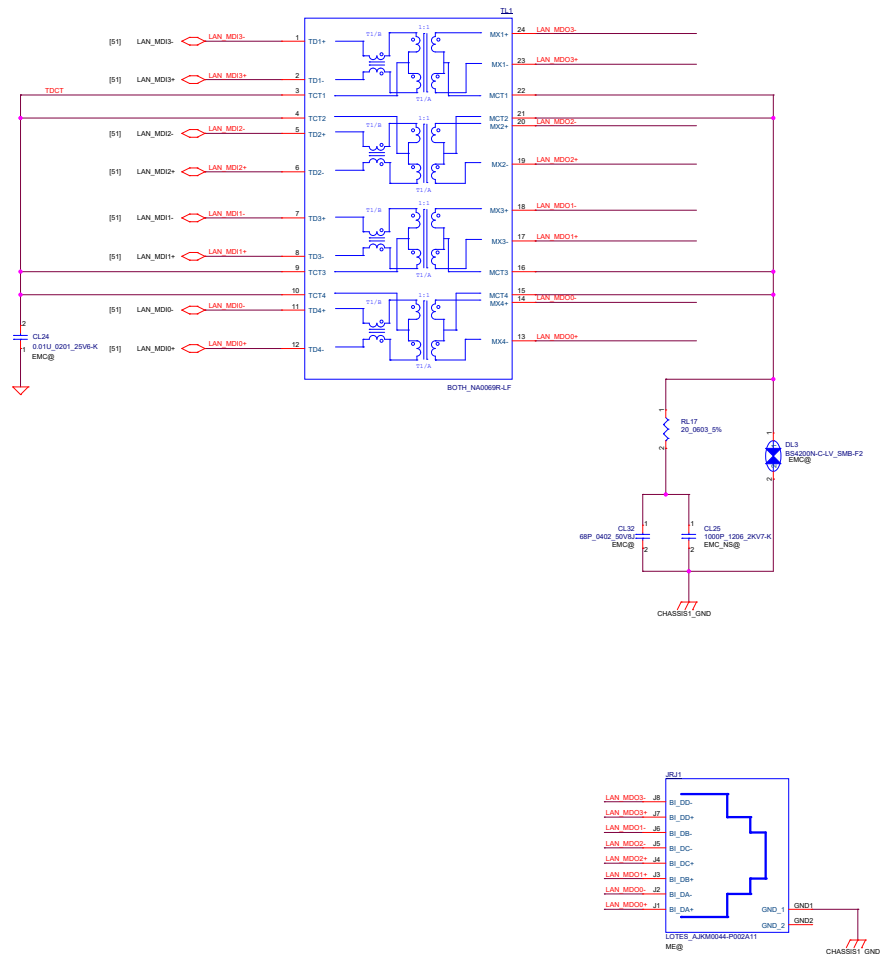
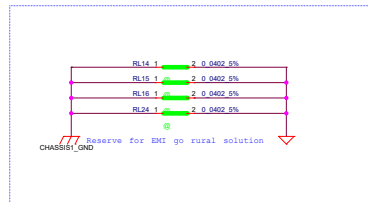
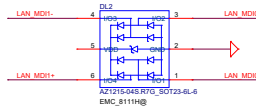
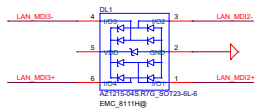
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2015/6/23	Deciphered Date	2015/6/23	USB2.0
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Rev	C	Document Number	EY515	
Rev	1.0	Rev	1.0	Rev
Rev	1.0	Rev	1.0	Rev



[illegible]



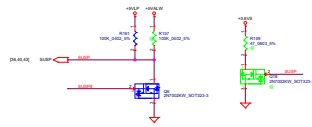
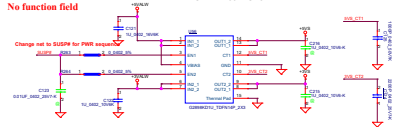
DL1/DL2
1'S PN:SC300005900
Place Close to TL1



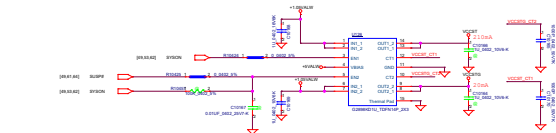
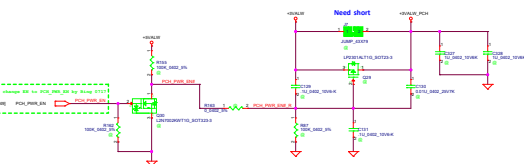
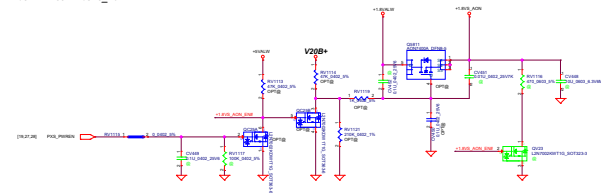
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/10/22	Deciphered Date	2014/10/22	LAN_Transformer	
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Size	Document Number	RYS15		Rev	
1	1	1.0		1.0	
DATE	Thursday, March 20, 2015	FILED	02	07	14

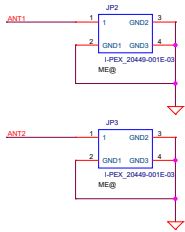
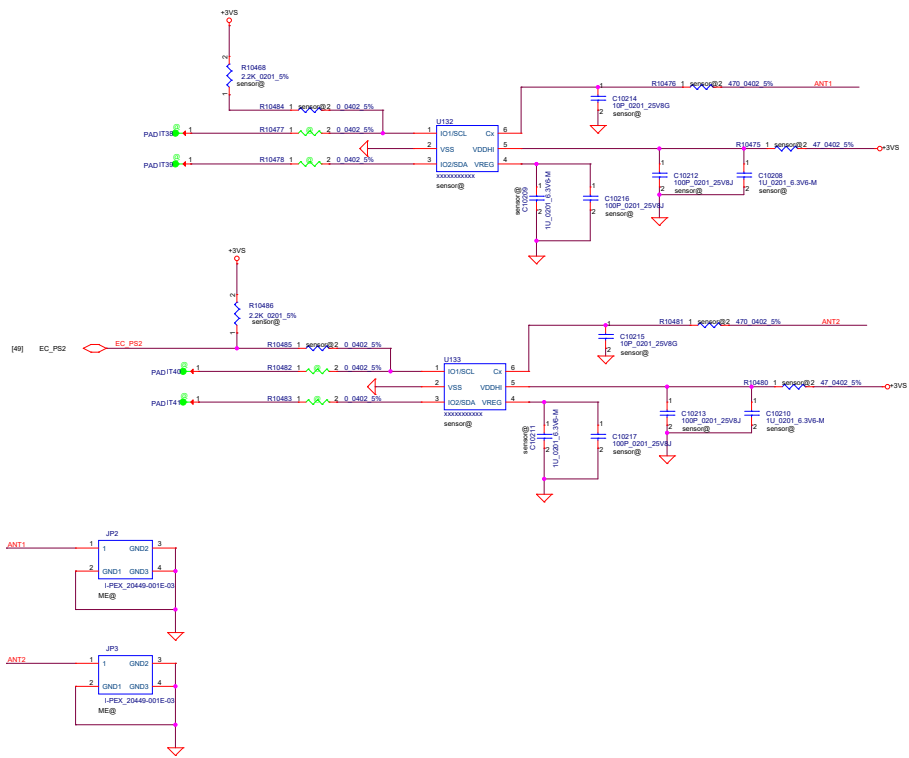
No function field

+5VALW to +5VS




+1.8VALW to +1.8VS_ACM

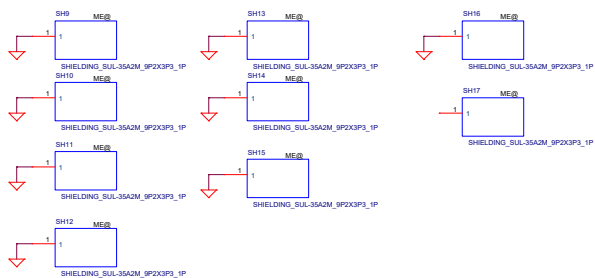
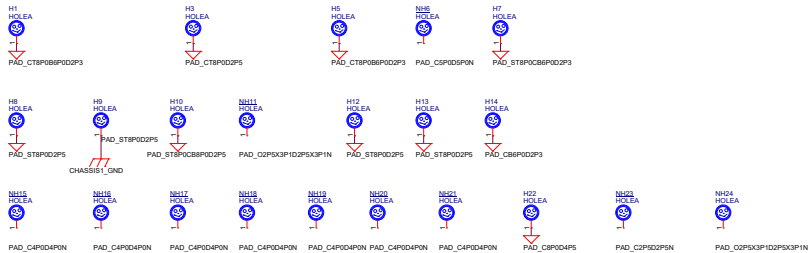




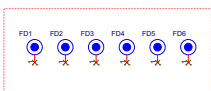
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				Version	March 20, 2015
				Sheet	54 of 74



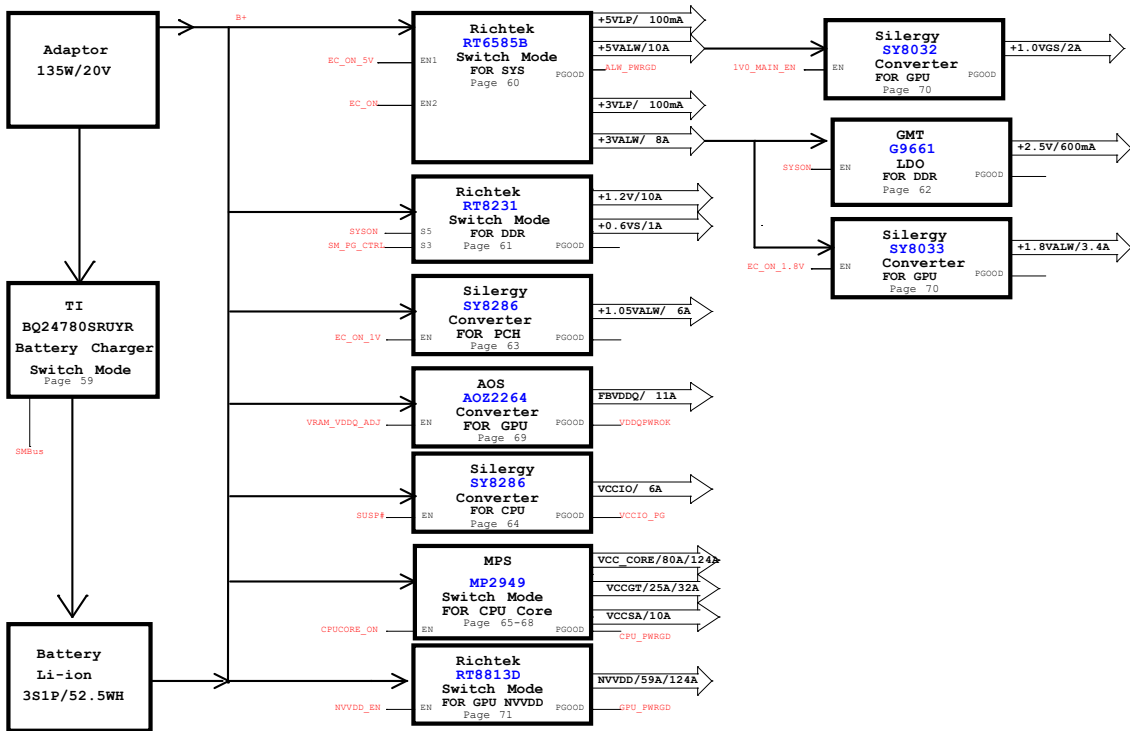
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Date			Friday, March 26, 2016	Sheet 05 of 74

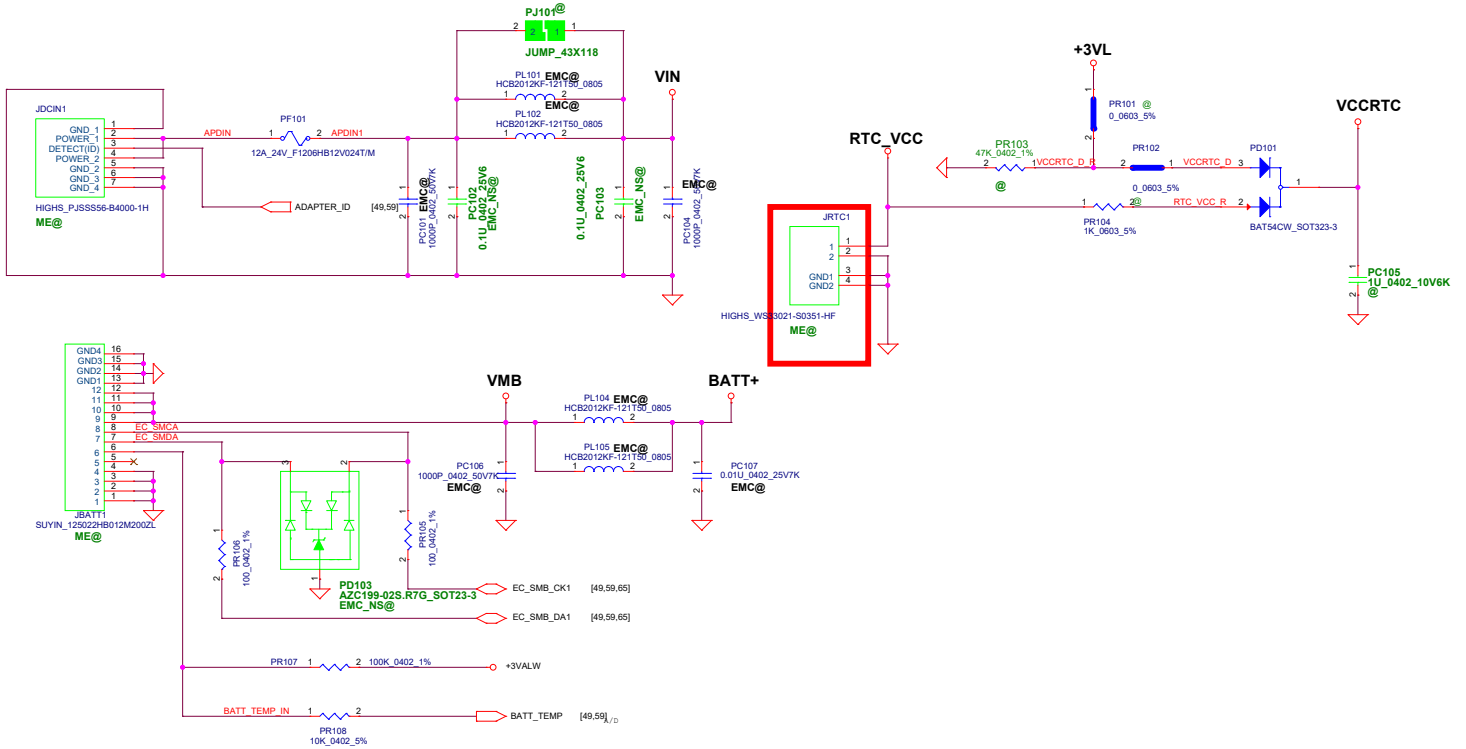


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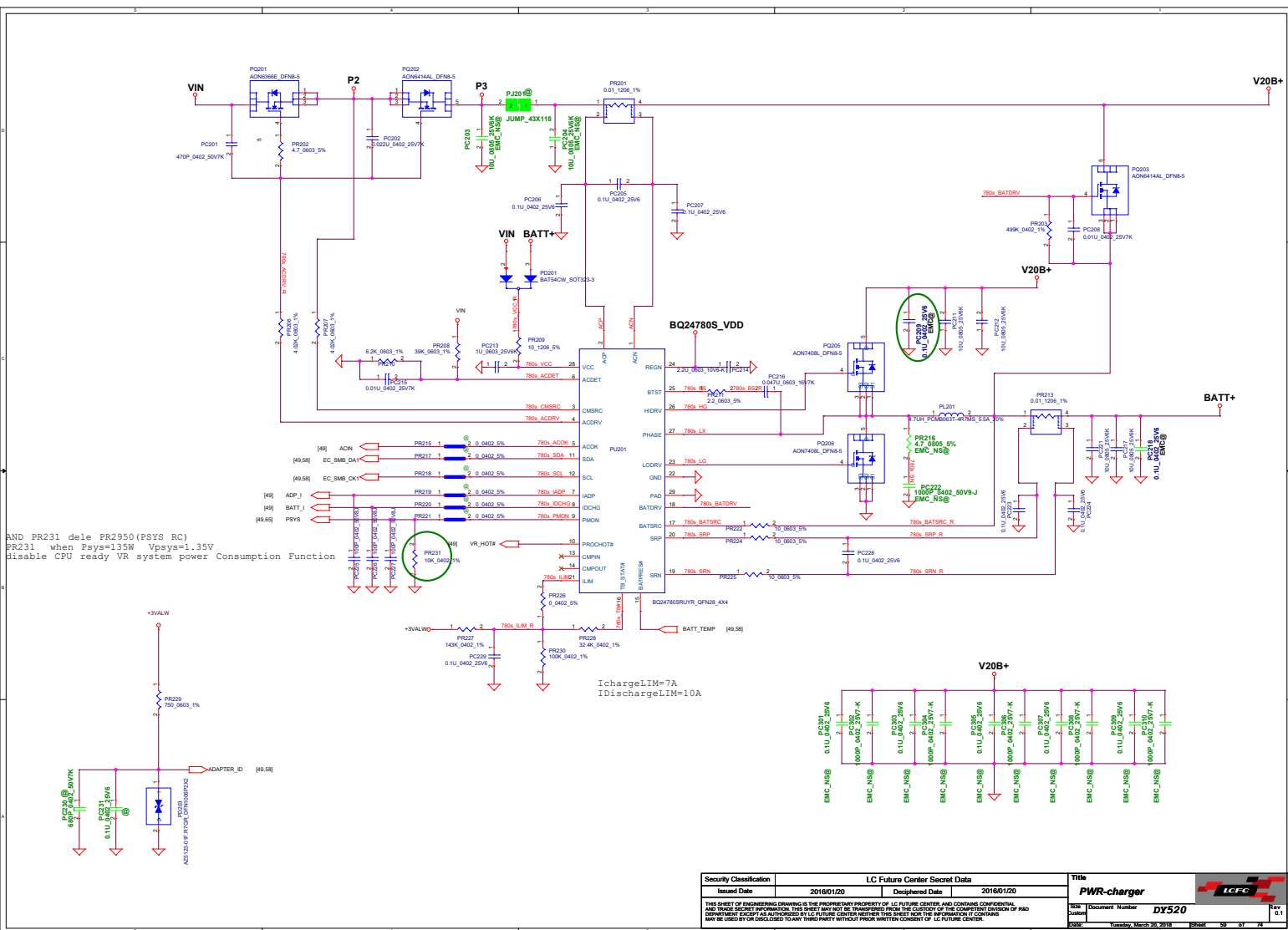


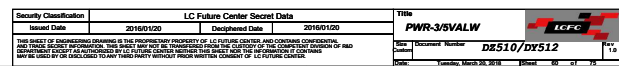
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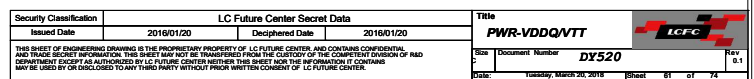


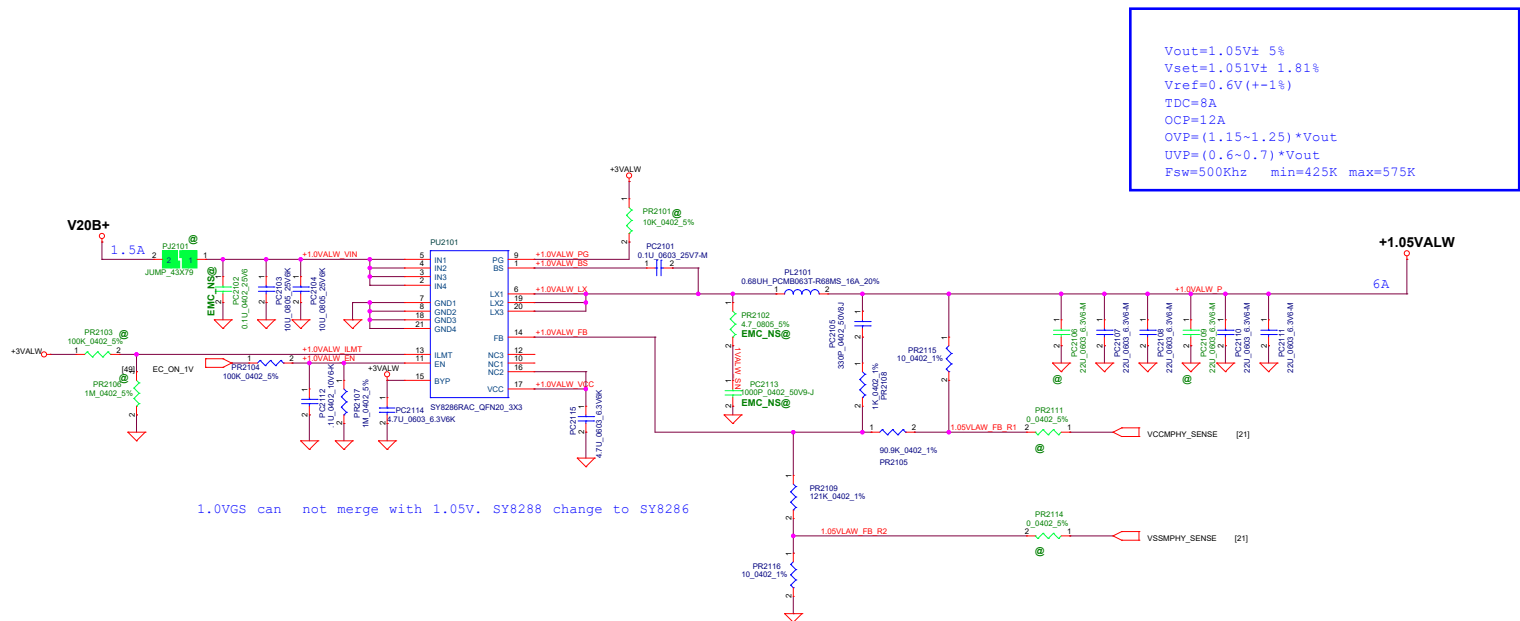


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				Sheet 58 of 74





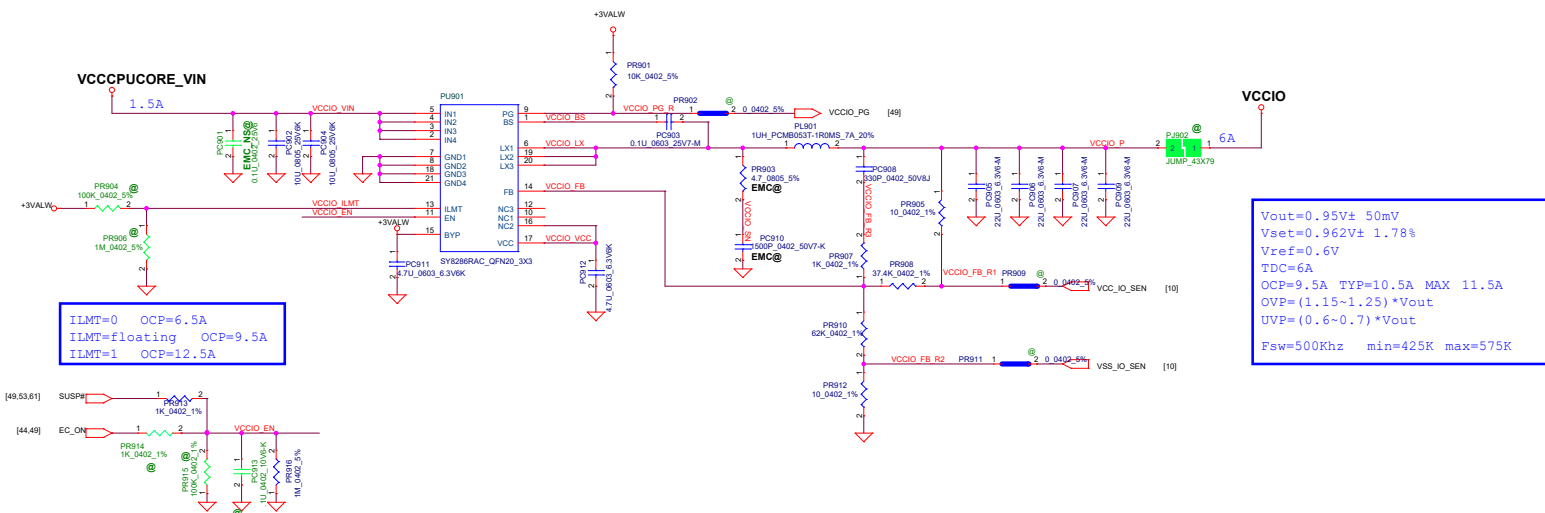





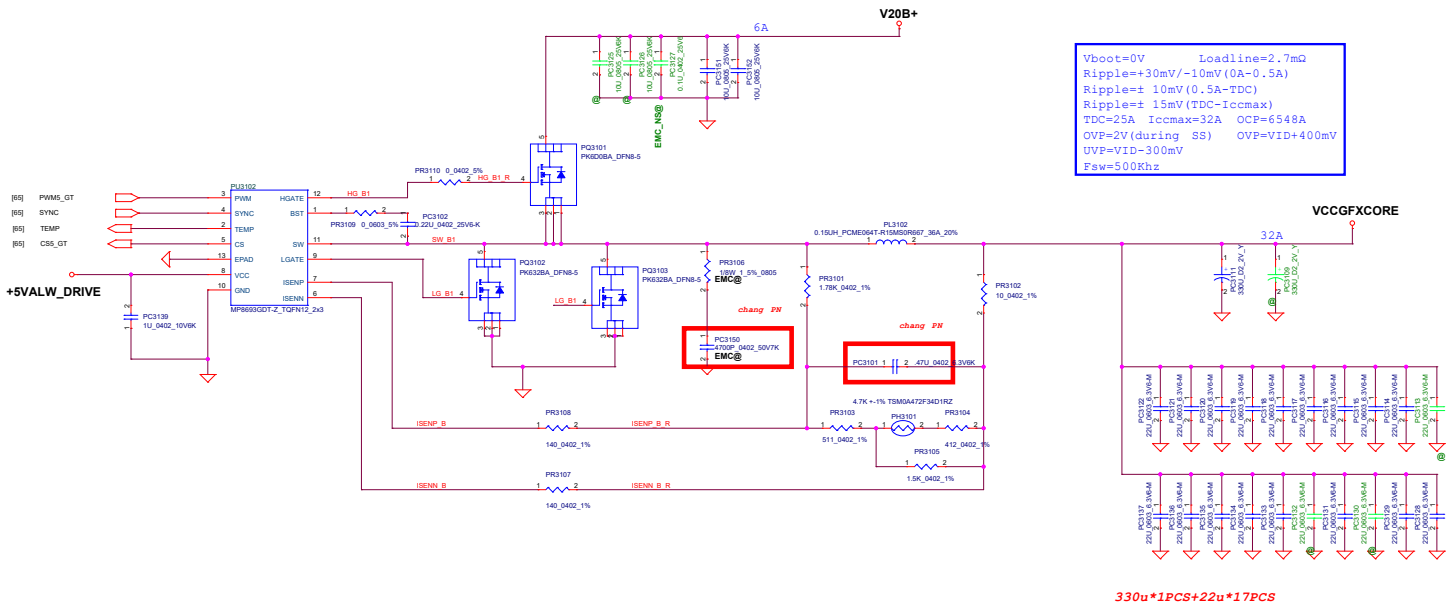
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Rev	Document Number	Rev
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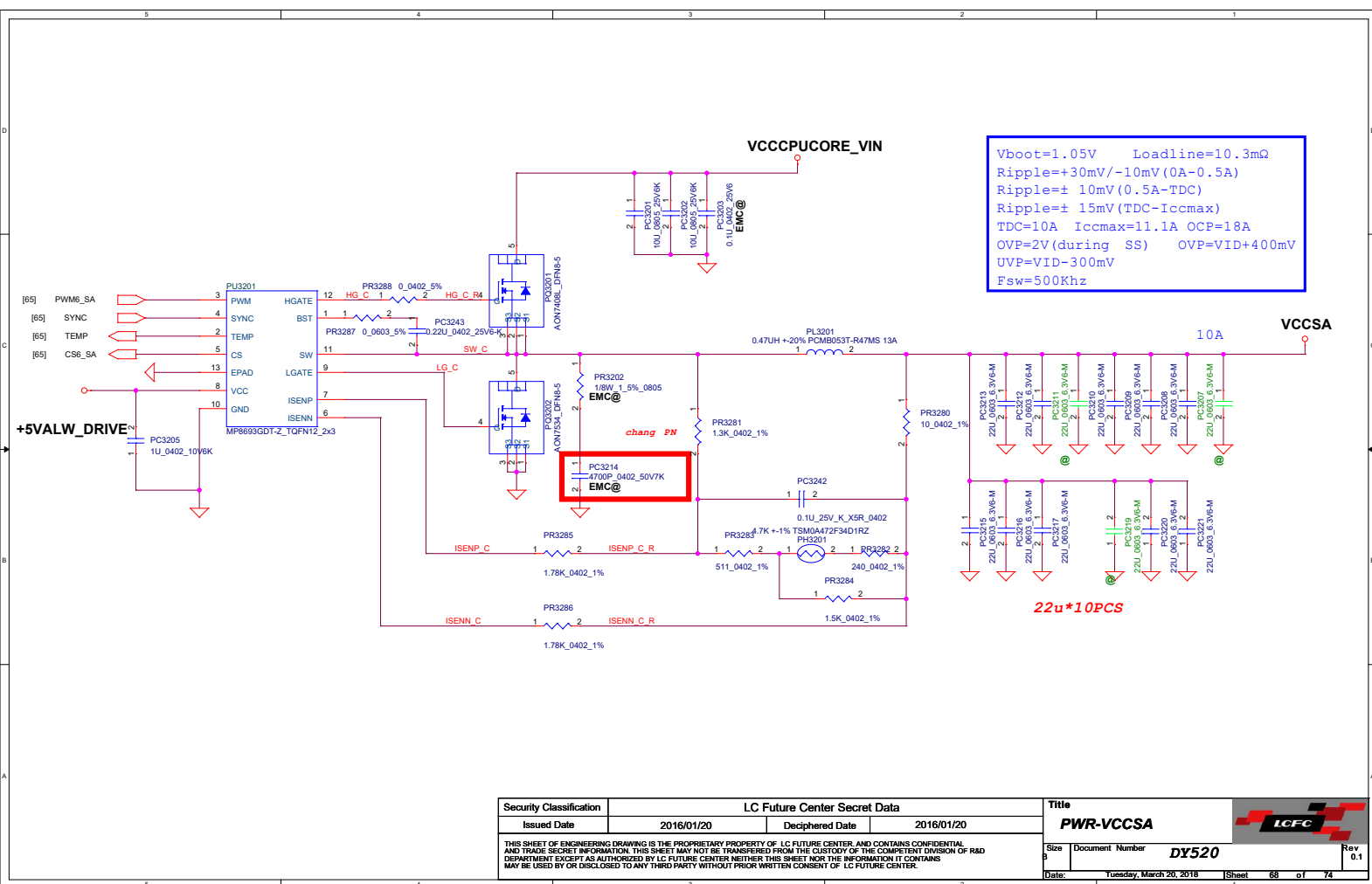
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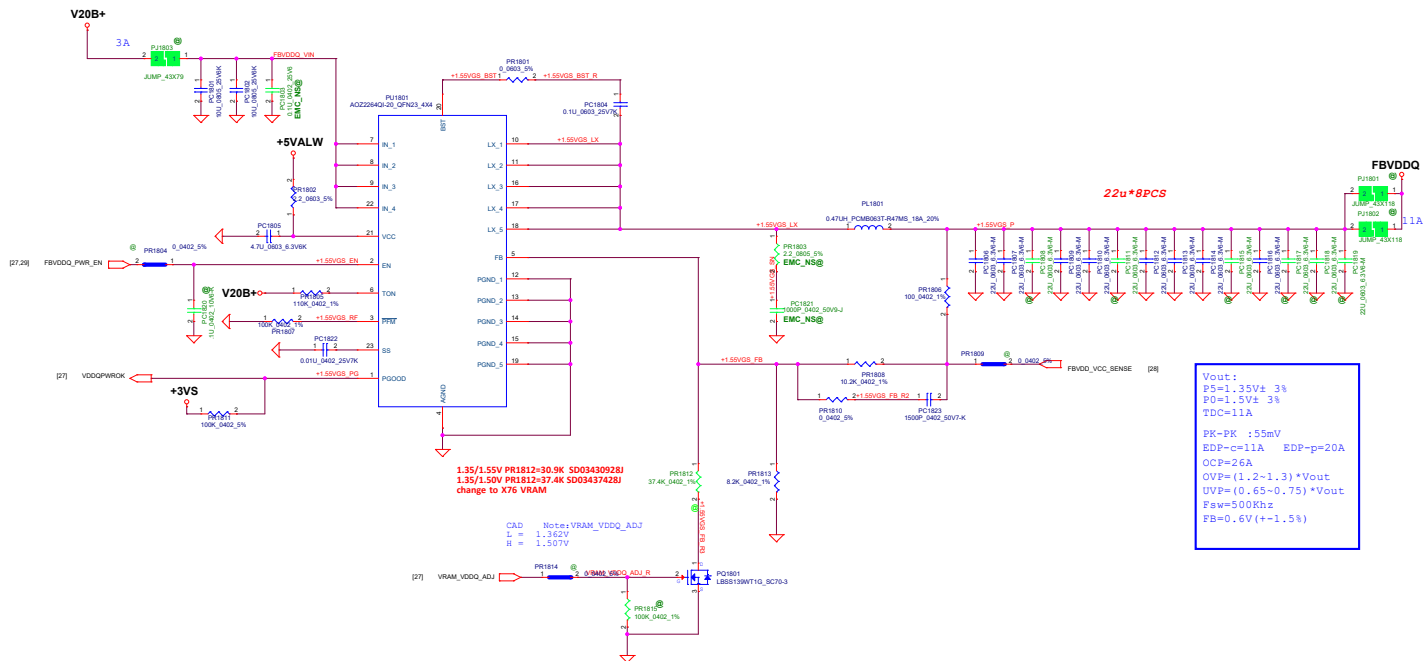


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Rev	1.0								
Date:	Tuesday, March 20, 2016			Sheet	64	of	74		



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				Sheet	87 of 94
				Rev	0.1





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Date		Tuesday, March 20, 2018		Sheet 38 of 14	

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